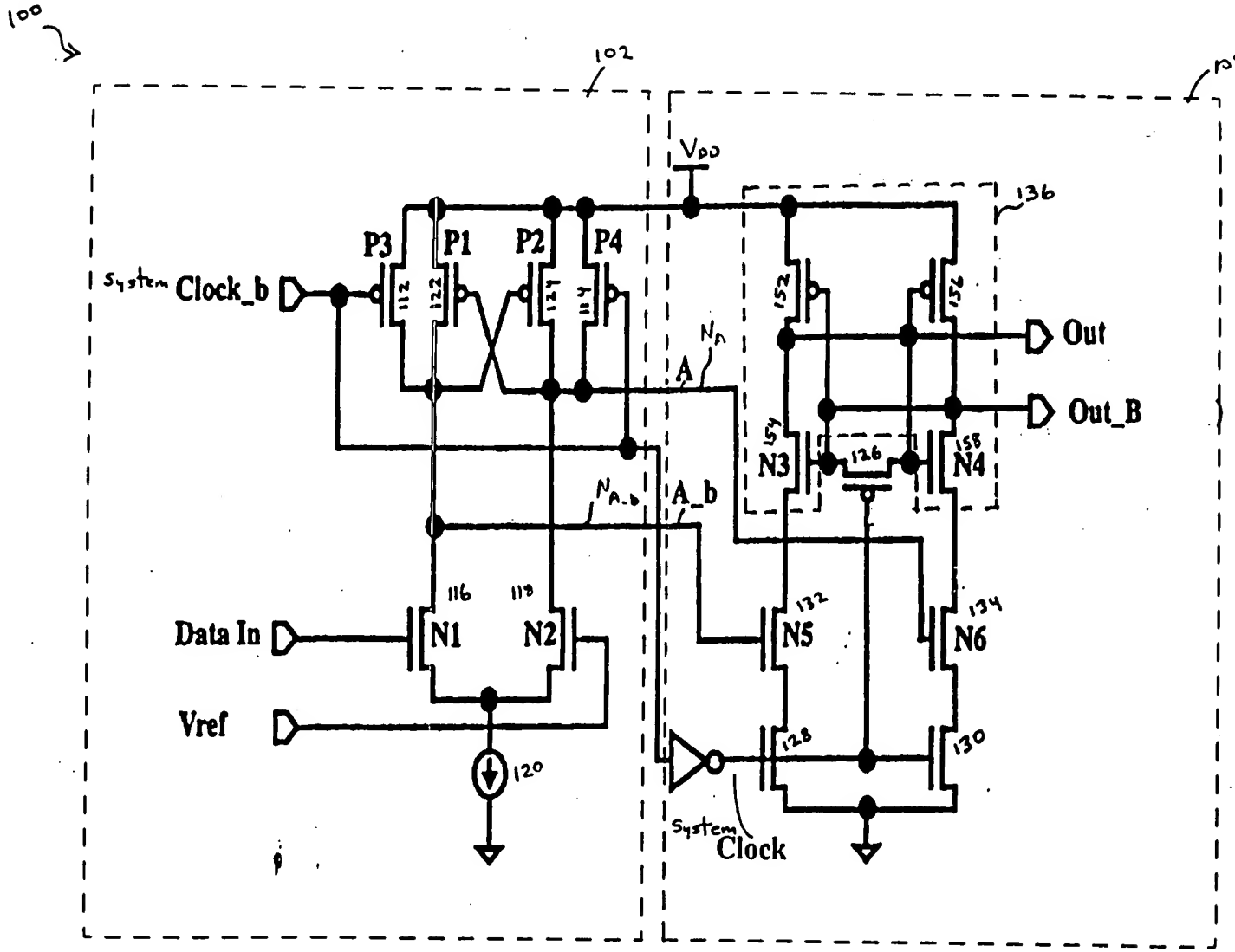
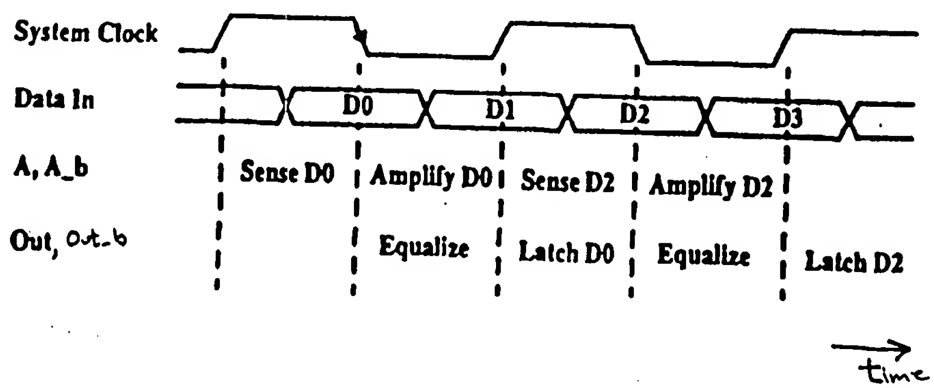


Prior Art

FIG 1



Prior Art

FIG. 2

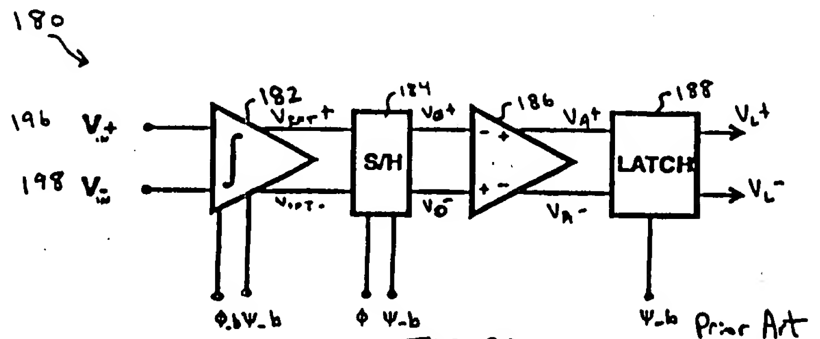

180
196
198
182
184
186
188
S/H
LATCH
Prior Art

FIG. 3A

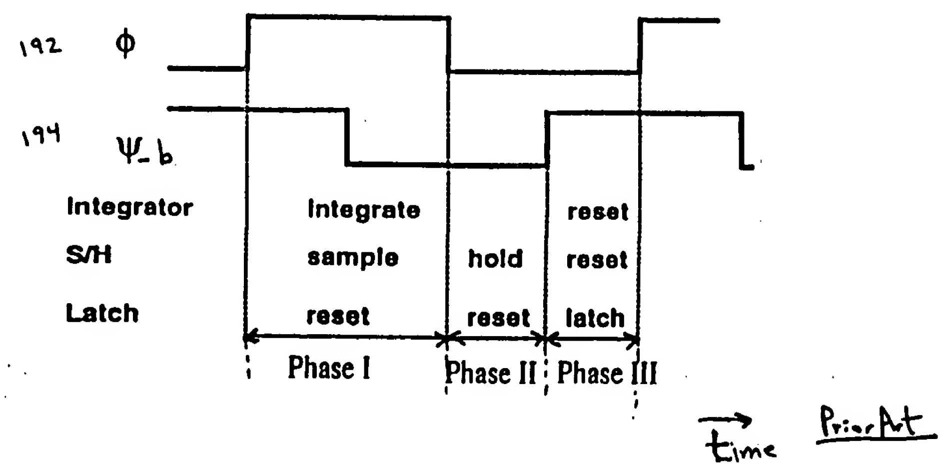
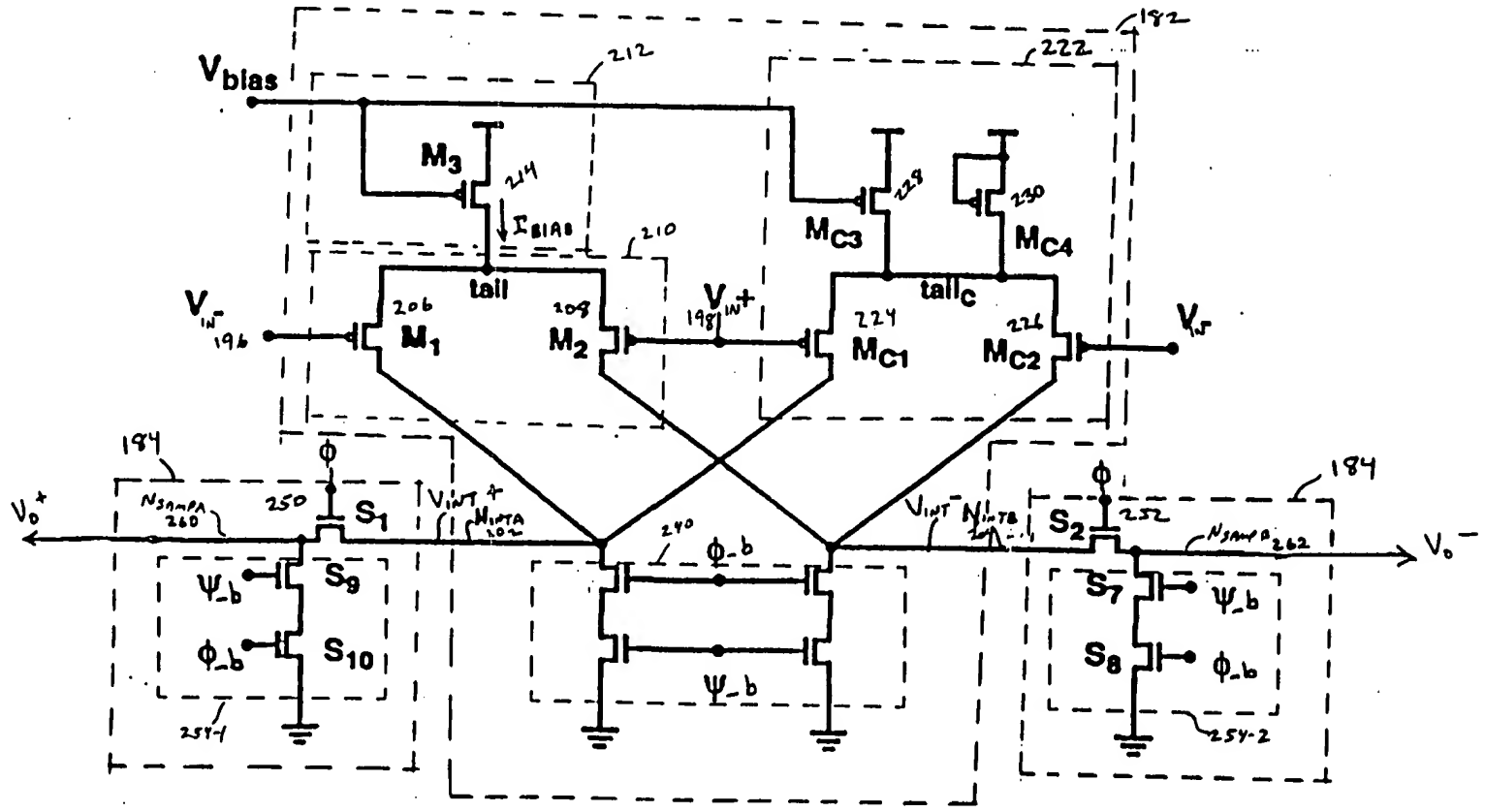

192
194
Integrator
S/H
Latch
Integrate
sample
reset
hold
reset
reset
reset
latch
Phase I
Phase II
Phase III
time
Prior Art

FIG. 3B



Prior Art

FIG. 4

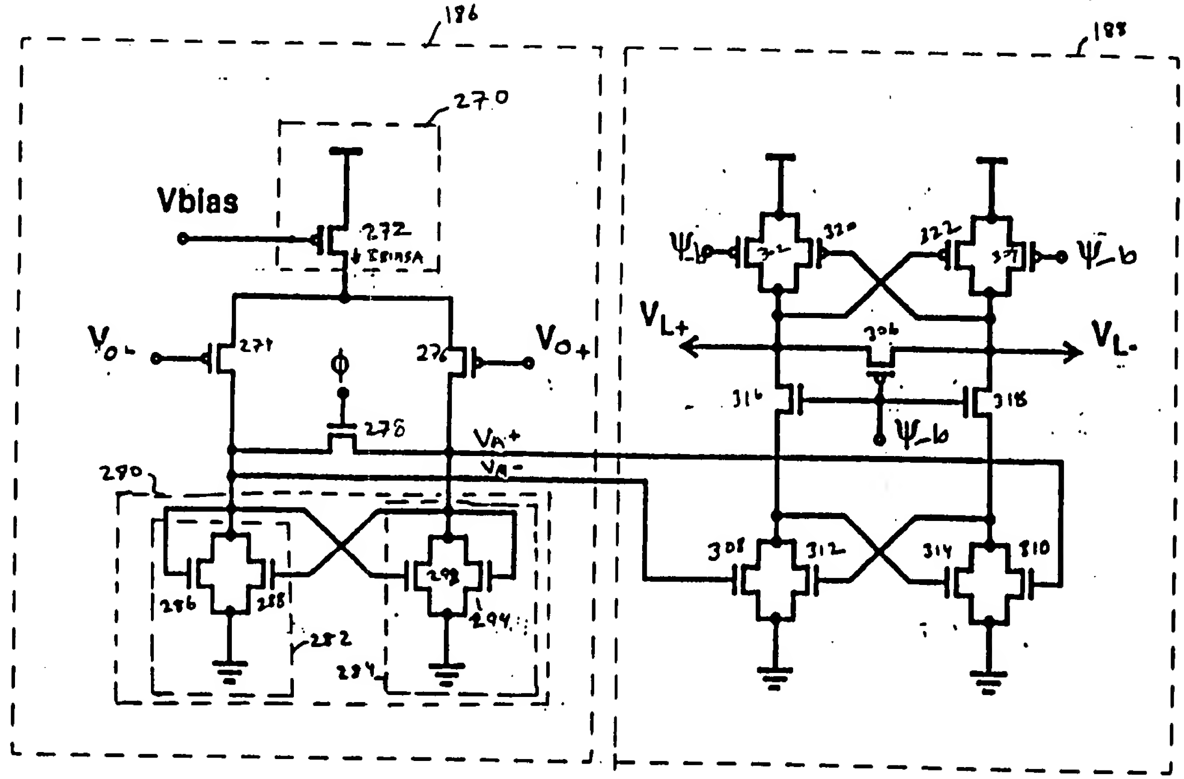


FIG. 5

Prior Art

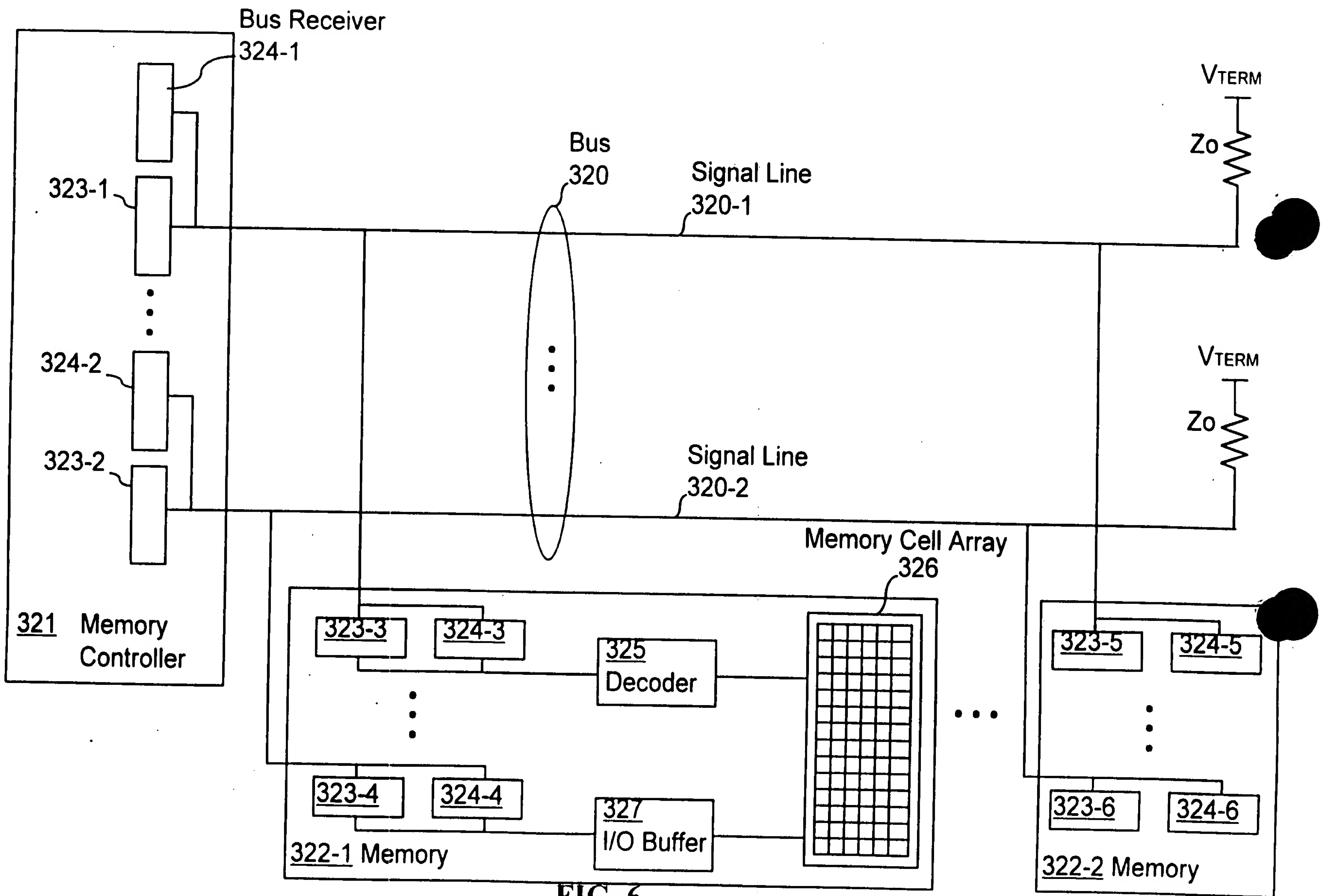


FIG. 6

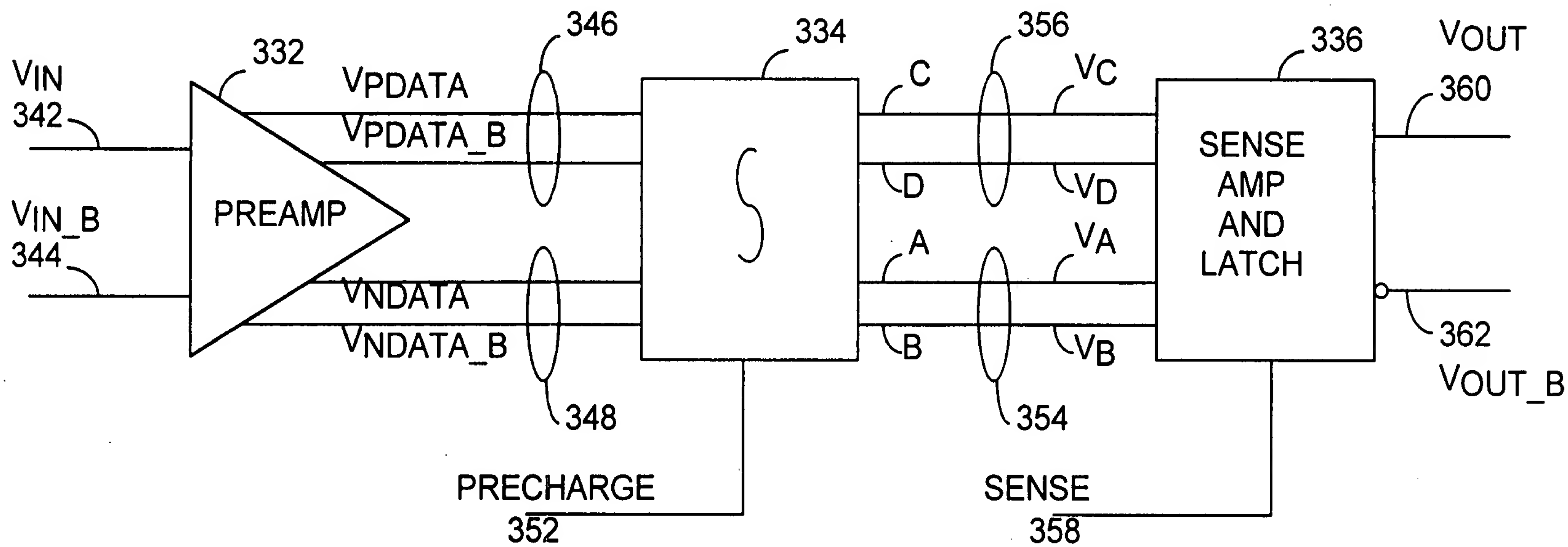

VIN
342
VIN_B
344
332
PREAMP
VPDATA
VPDATA_B
VNDATA
VNDATA_B
346
348
334
PRECHARGE
352
C
D
A
B
356
354
VC
VD
VA
VB
336
SENSE
AMP
AND
LATCH
SENSE
358
VOUT
360
362
VOUT_B

FIG. 7A

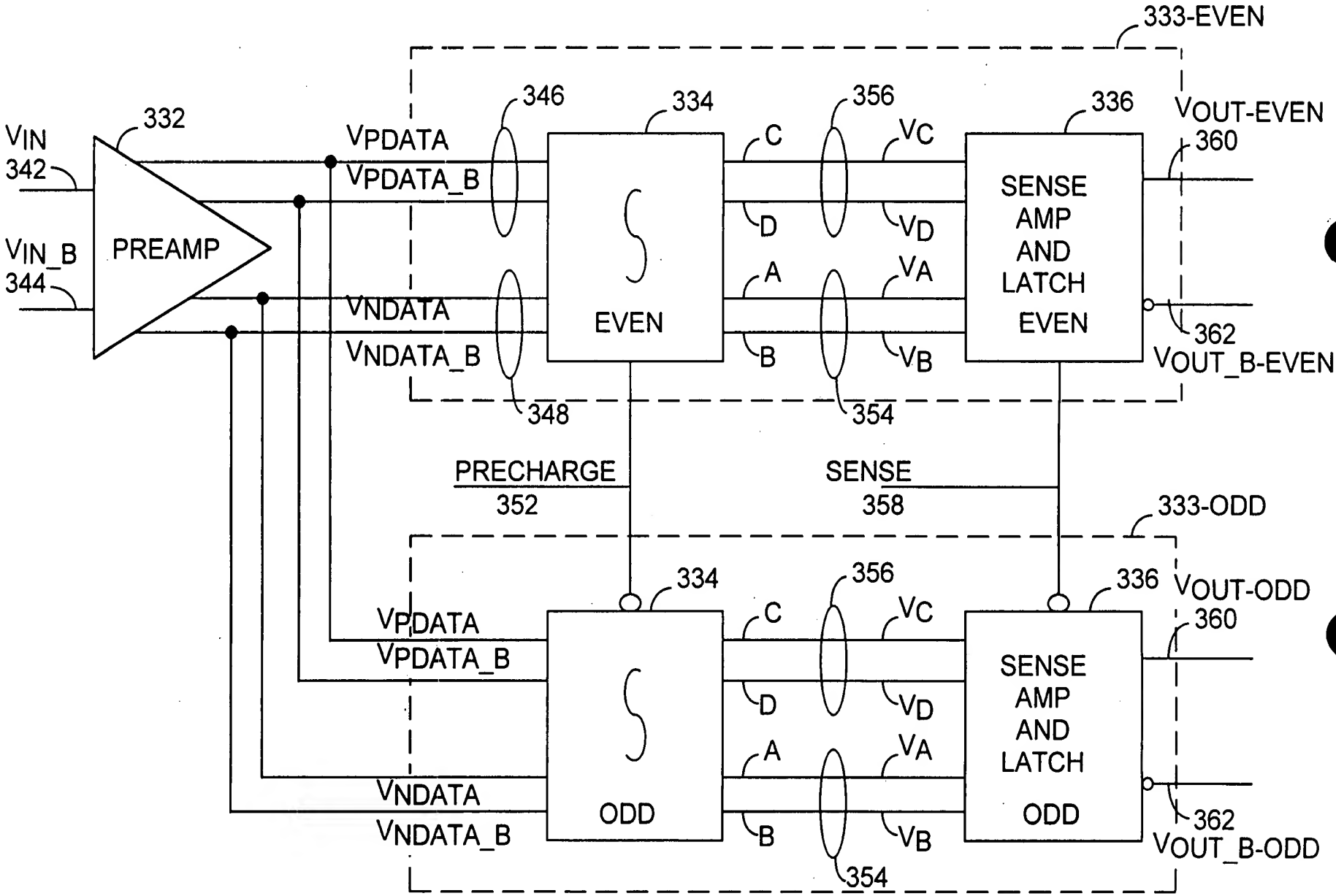


FIG. 7B

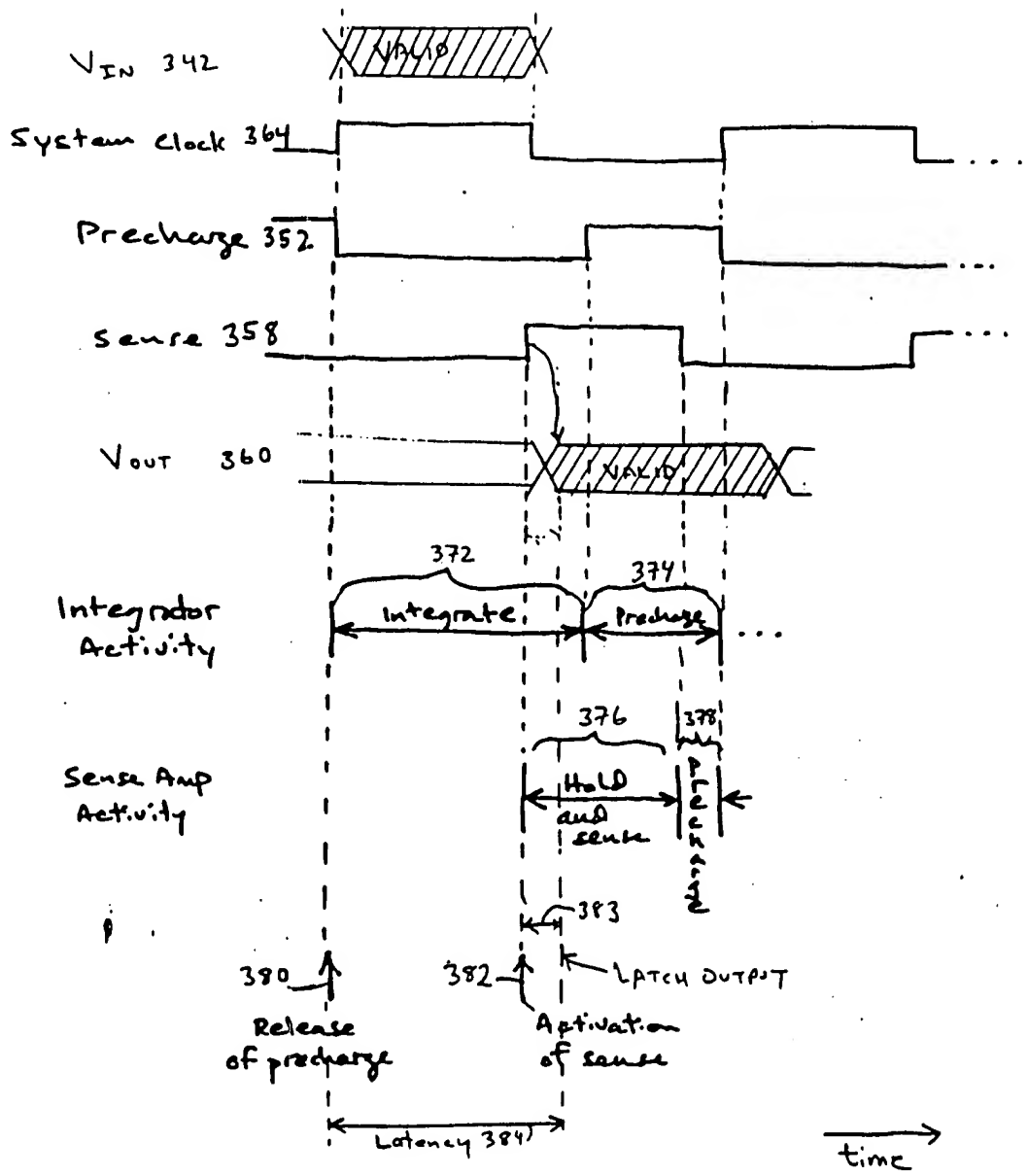

V_{IN} 342
System clock 364
Precharge 352
Sense 358
V_{OUT} 360
Valid
372
374
Integrate
Precharge
Integrator Activity
376
378
Hold and sense
Precharge
Sense Amp Activity
383
380
382
Latch Output
Release of precharge
Activation of sense
Latency 384
time

FIG. 8

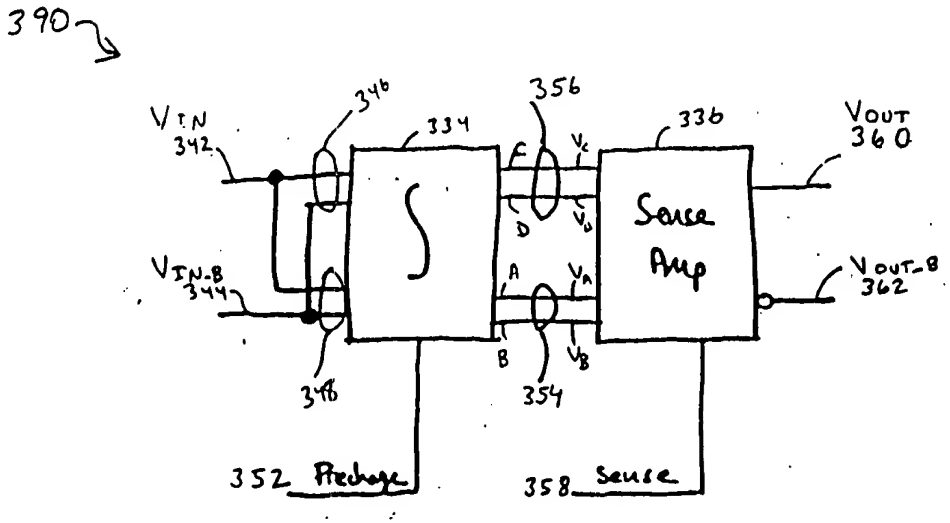


FIG. 9

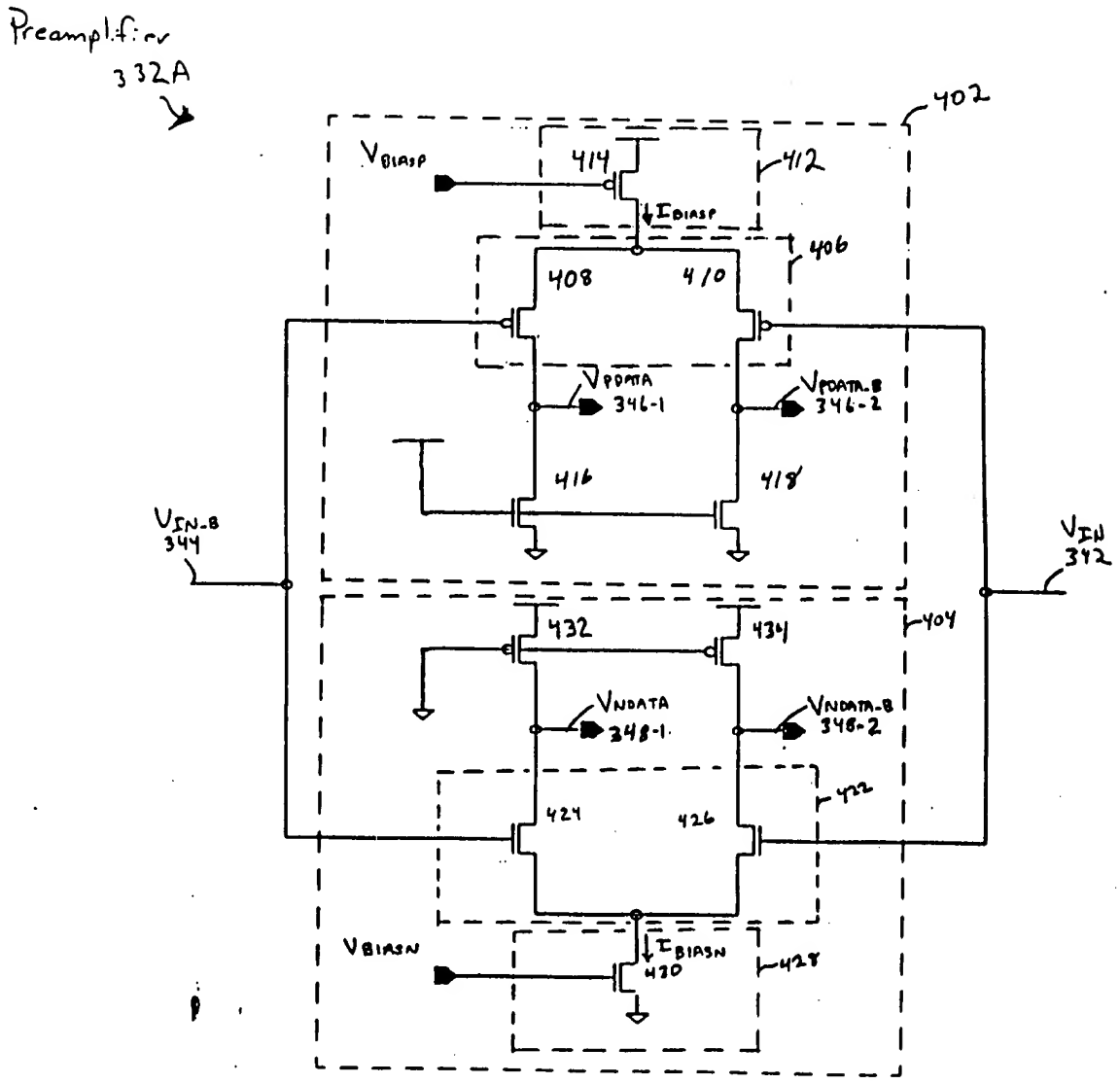


FIG. 10

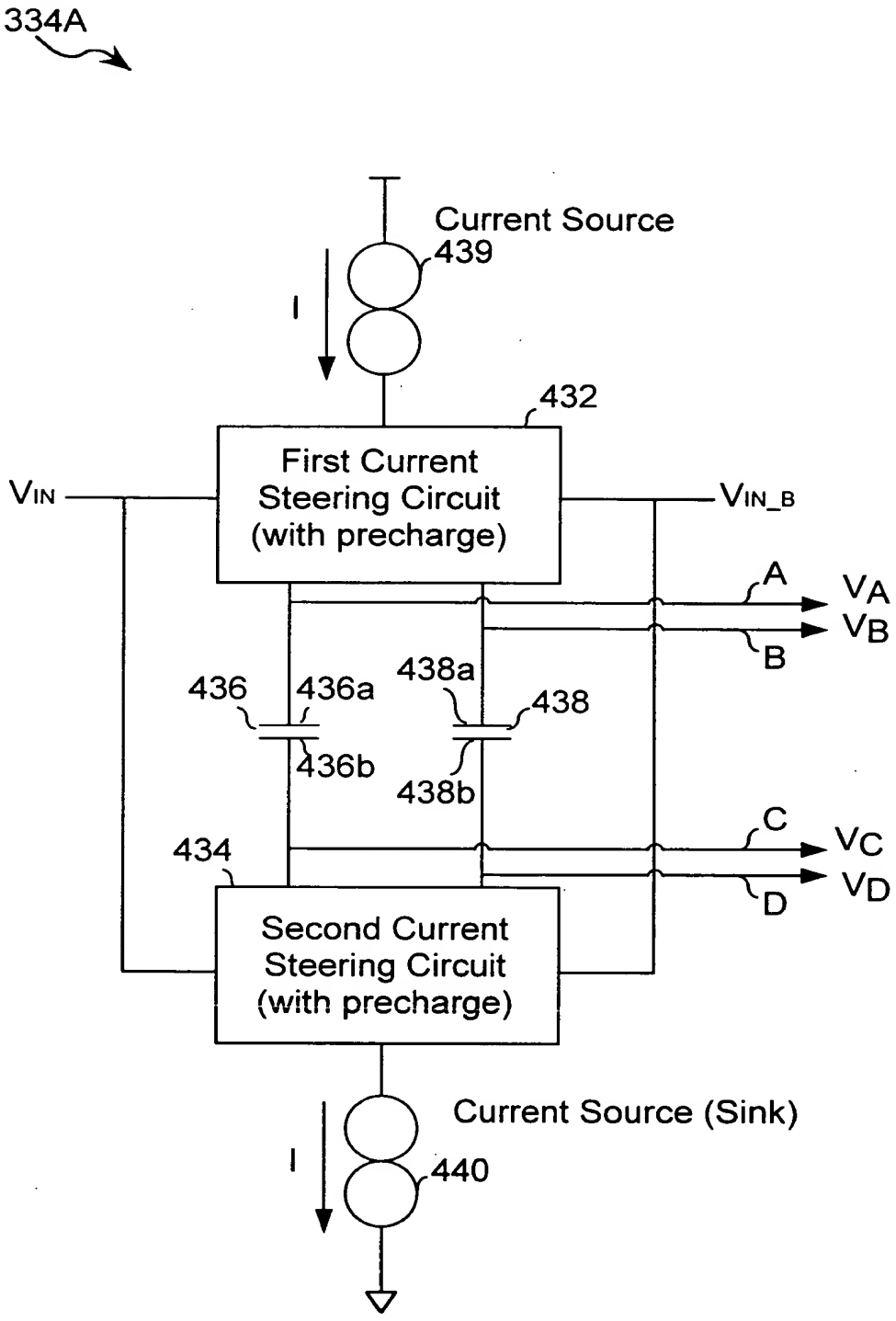

334A
Current Source
439
I
432
First Current
Steering Circuit
(with precharge)
VIN
VIN_B
A
VA
VB
B
436
436a
438a
438
436b
438b
C
VC
434
VD
D
Second Current
Steering Circuit
(with precharge)
Current Source (Sink)
I
440

FIG. 11A

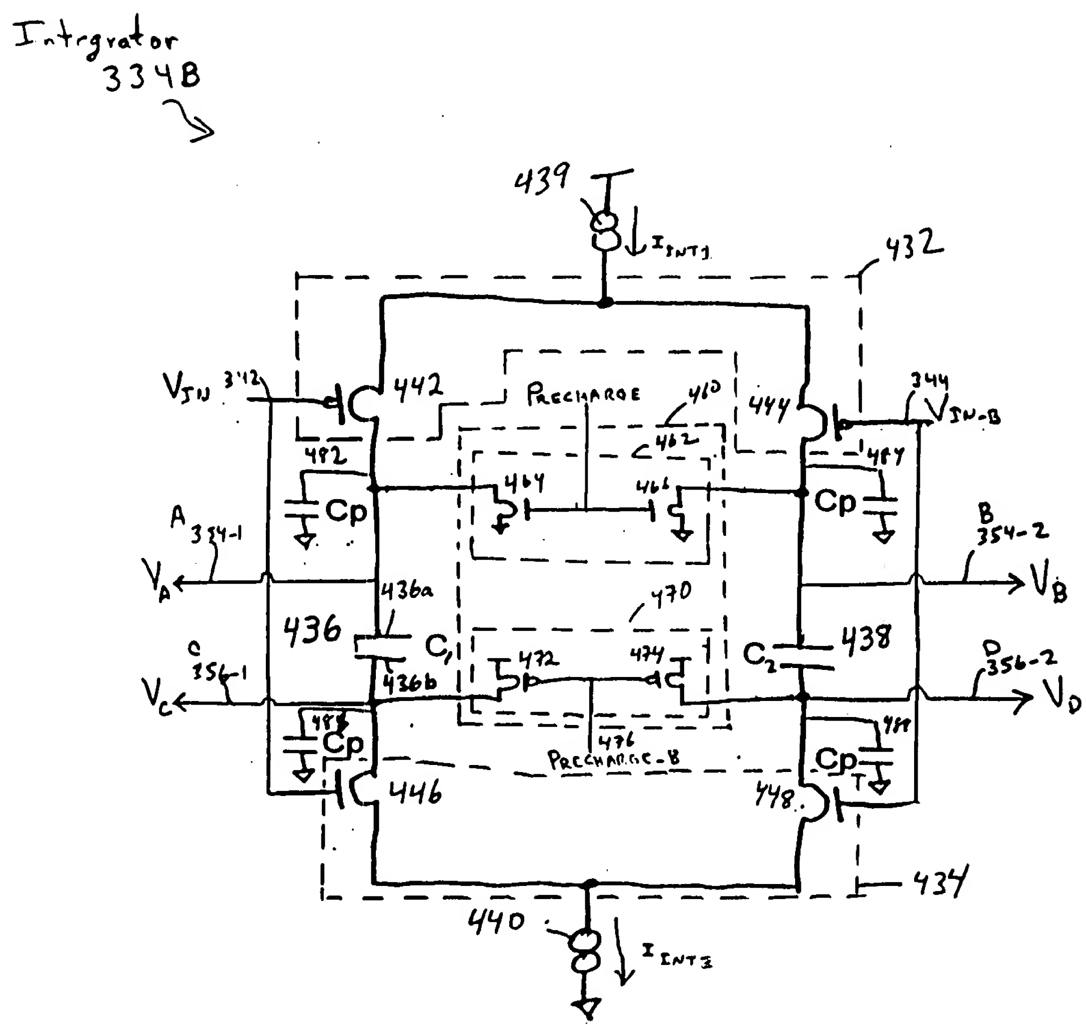

Intrgrator
334B
439
I_{INT1}
432
V_{IN} 342
442
PRECHARGE
460
444
344 V_{IN-B}
482
462
464
466
484
Cp
Cp
A 354-1
V_A
B 354-2
V_B
436a
470
436
C_1
C 356-1
V_C
436b
472
474
C_2
438
D 356-2
V_D
488
Cp
476
PRECHARGE-B
486
Cp
446
448
434
440
I_{INT2}

FIG. 11B

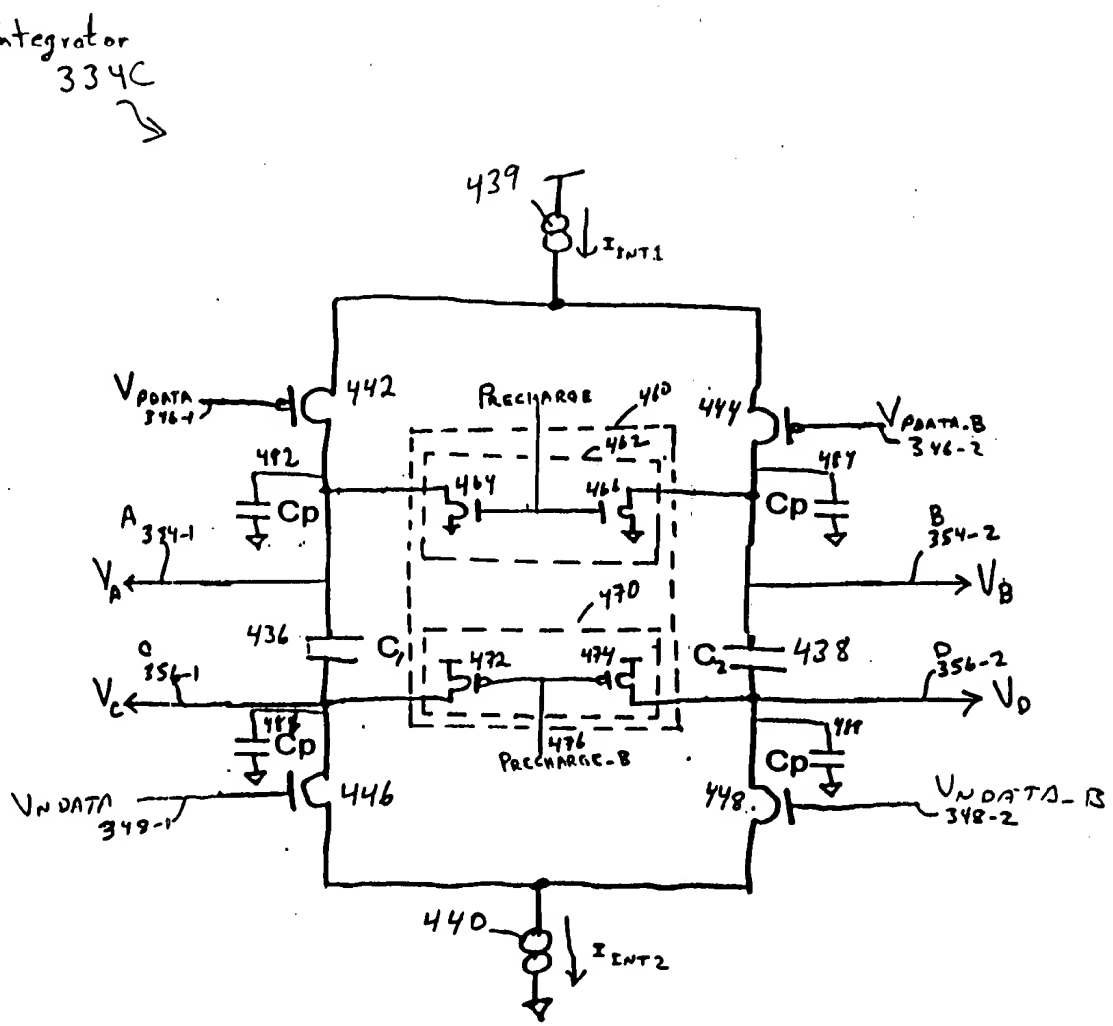


FIG. 11C

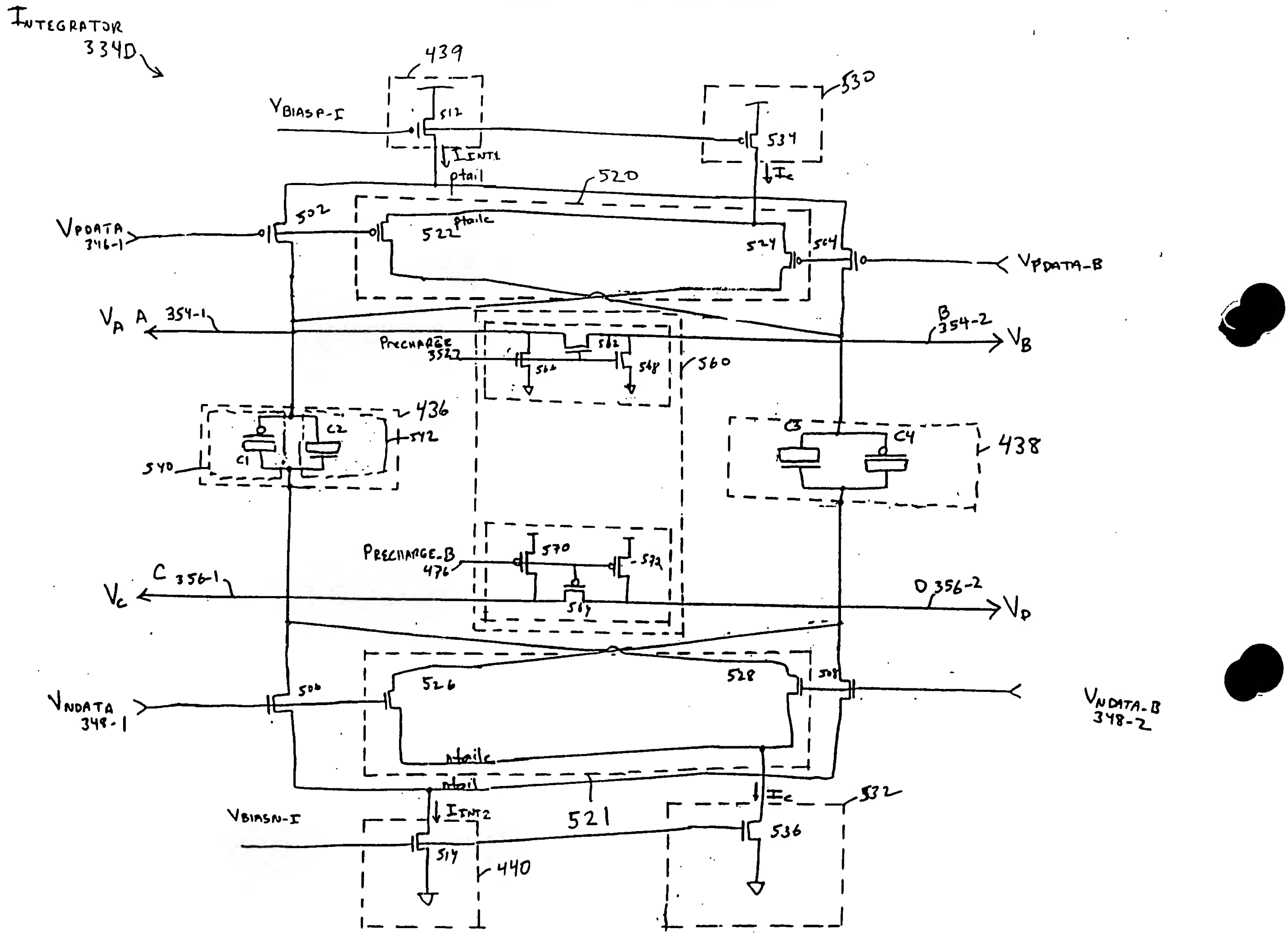


FIG. 12

Integrator
334E

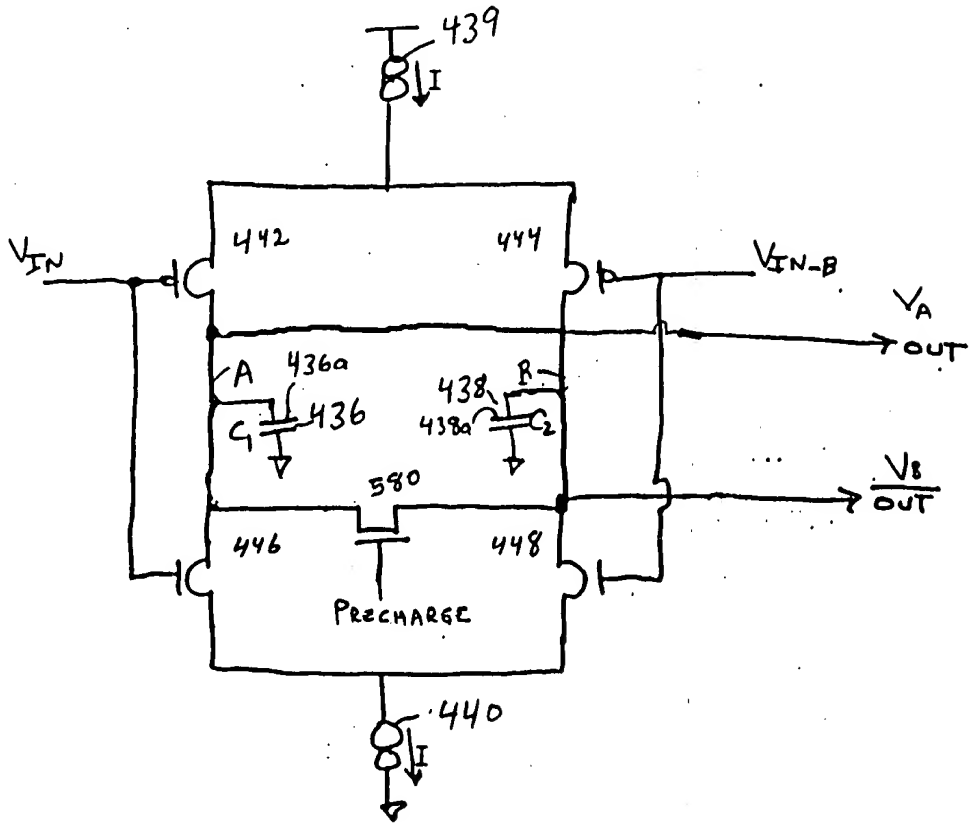


FIG. 13

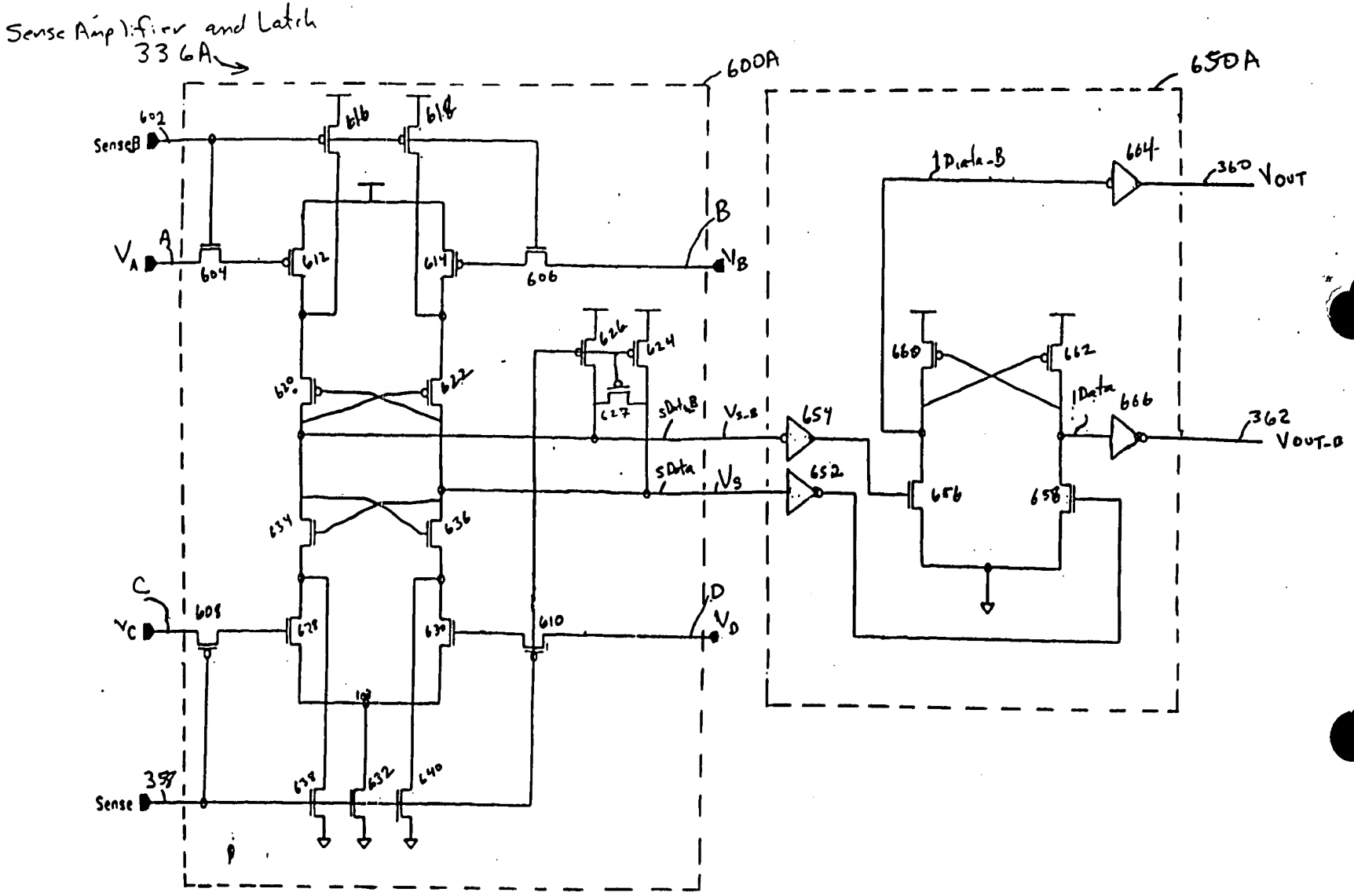

Sense Amplifier and Latch
336A
600A
650A
602
SenseB
616
618
B
V_B
V_A
A
604
612
614
606
626
624
620
622
627
sDataB
V_{S_B}
654
sData
V_S
652
634
636
C
V_C
608
628
630
610
D
V_D
632
640
Sense
660
662
DataB
664
360
V_{OUT}
Data
666
362
V_{OUT_B}
656
658

FIG. 14A

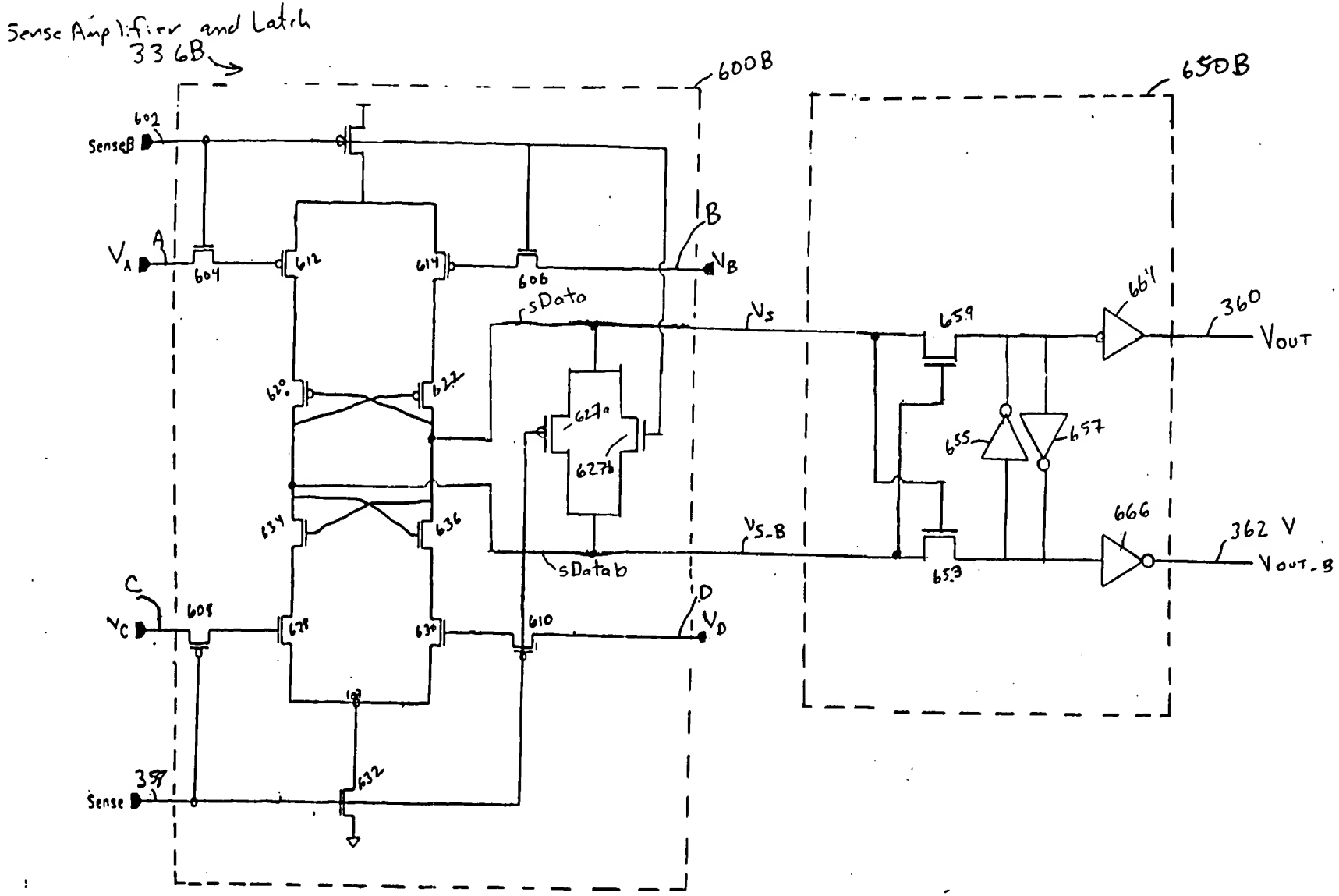


FIG. 14B

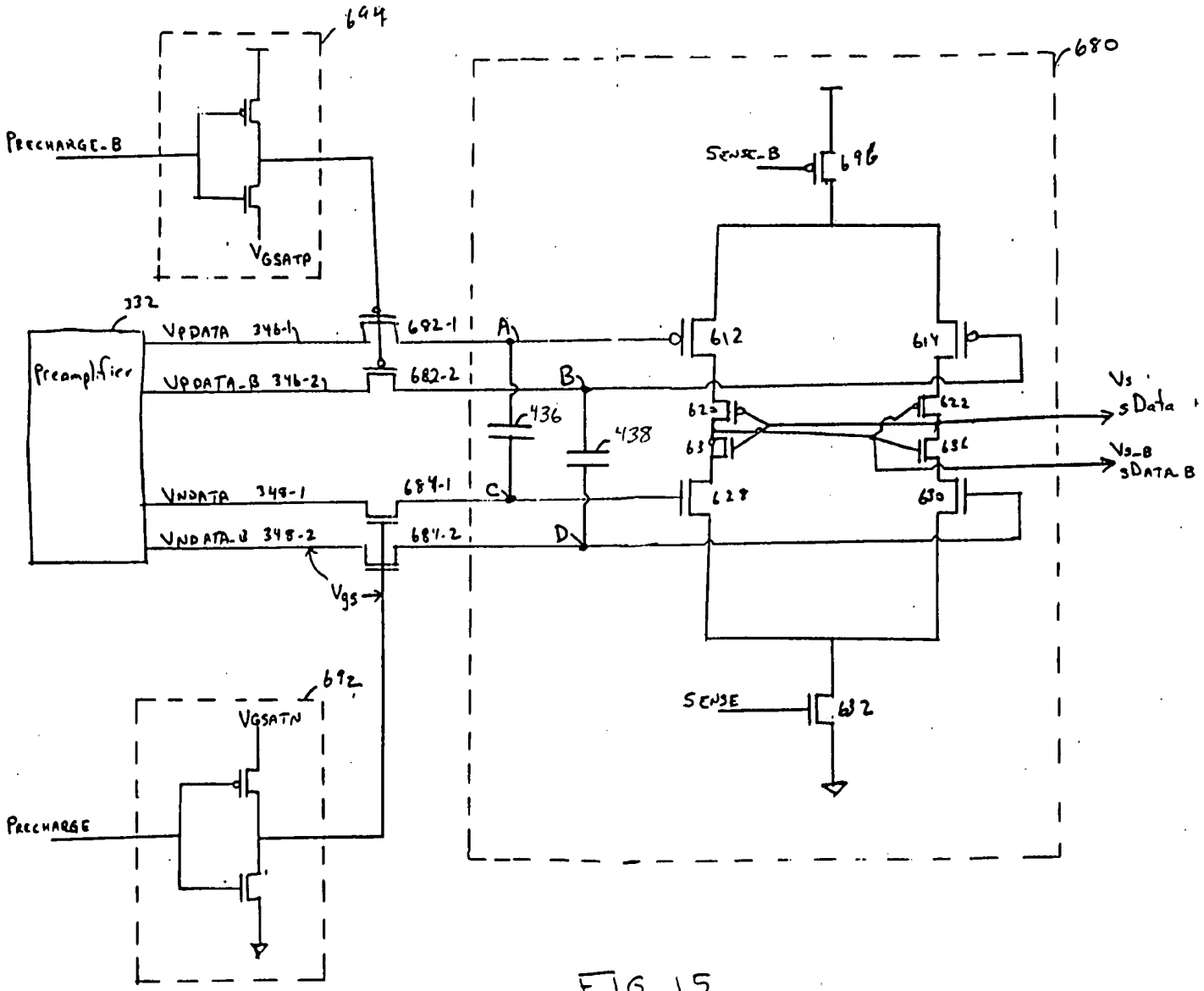

694
PRECHARGE_B
VGSATP
680
SENSE_B
696
332
Preamplifier
VPDATA 346-1
VPDATA_B 346-2
682-1
682-2
A
B
436
438
612
614
622
626
630
632
Vs sData
Vs_B sDATA_B
VNDATA 346-1
VNDATA_B 348-2
684-1
684-2
C
D
Vgs
692
VGSATN
PRECHARGE
SENSE

FIG. 15

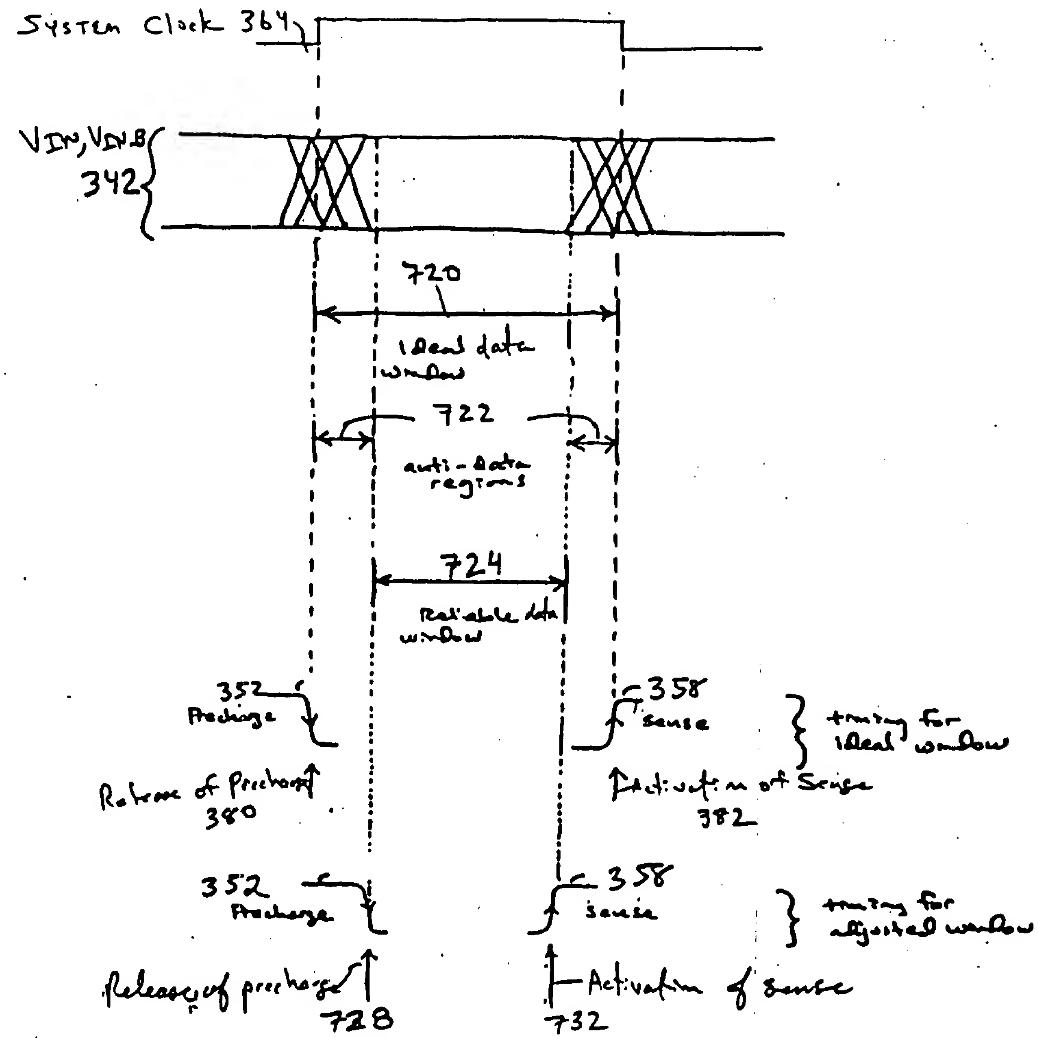


FIG. 16

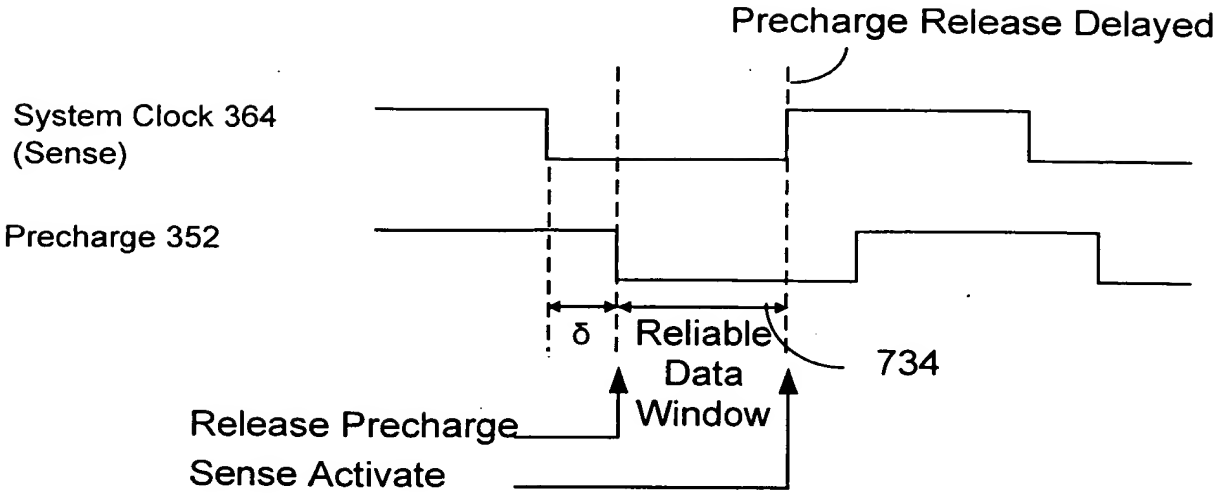


FIG. 17A

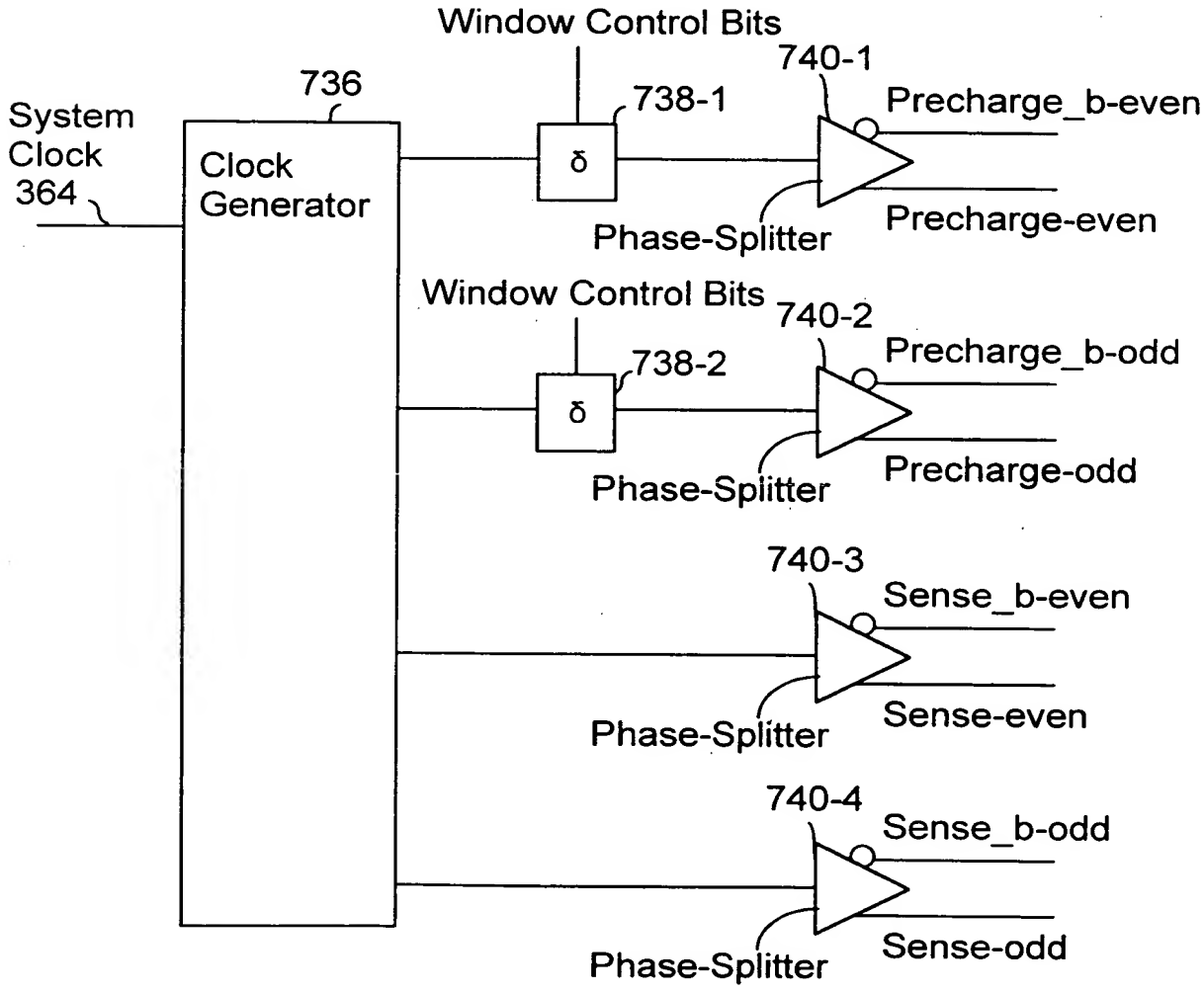
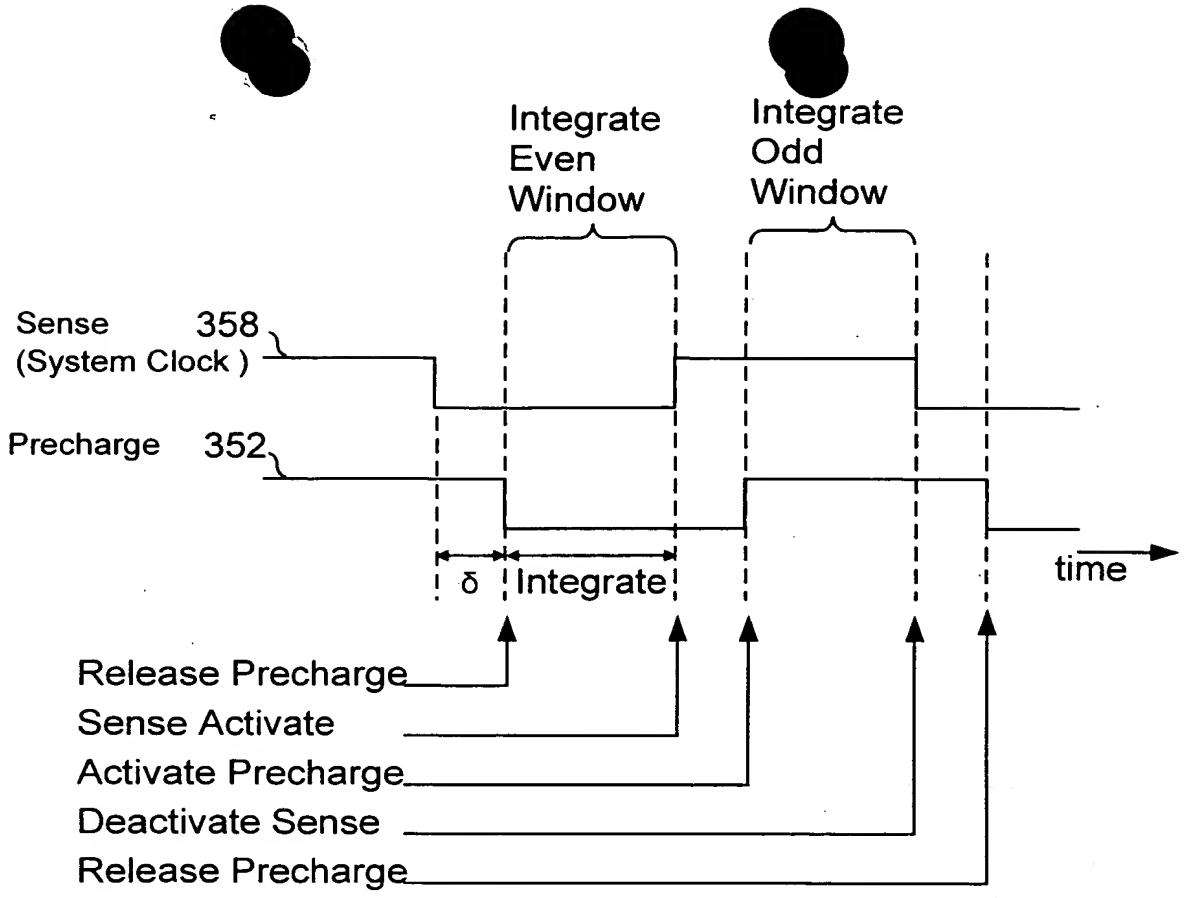
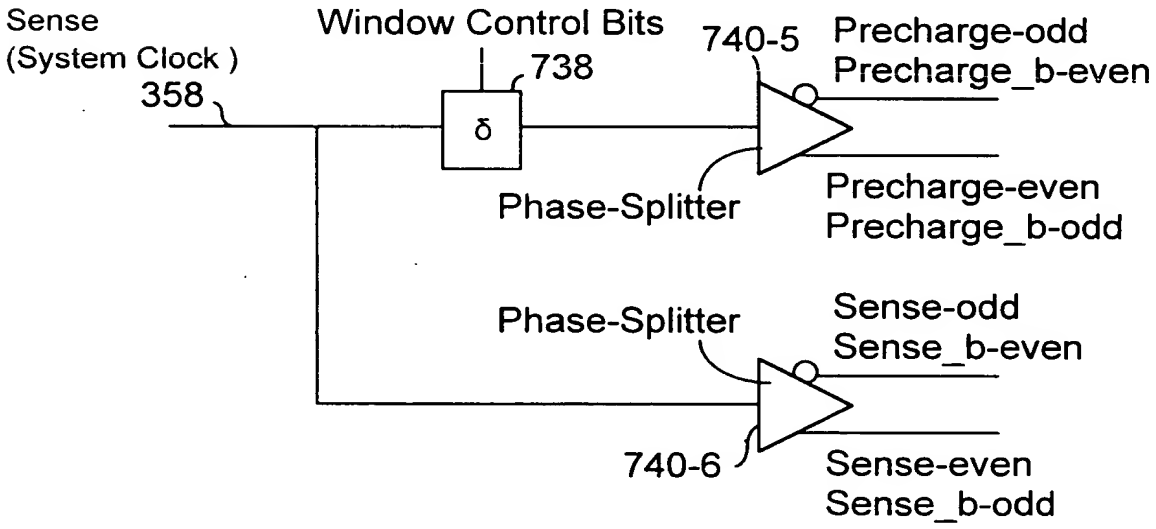


FIG. 17B



Timing Diagram of Precharge and Sense Signals

FIG. 17C



Circuit for Timing Diagram of Fig.17C

FIG. 17D

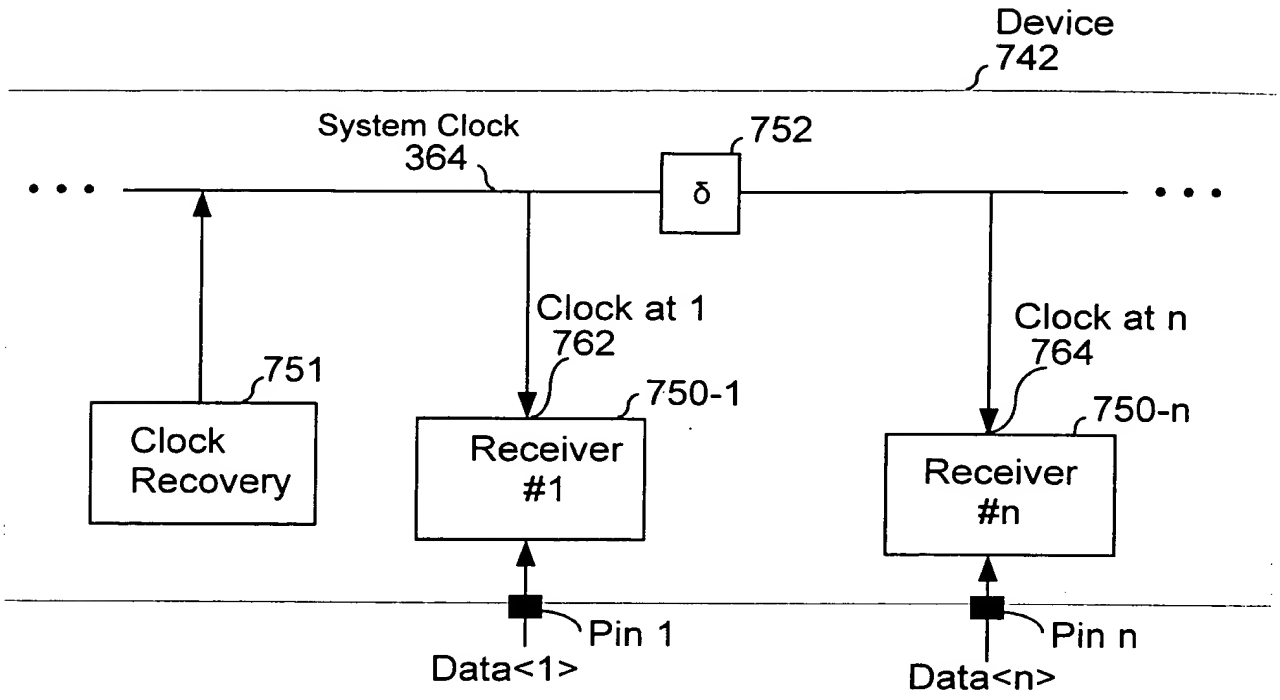

Device
742
System Clock
364
752
δ
Clock at 1
762
Clock at n
764
751
750-1
750-n
Clock
Recovery
Receiver
#1
Receiver
#n
Pin 1
Pin n
Data<1>
Data<n>

FIG. 18

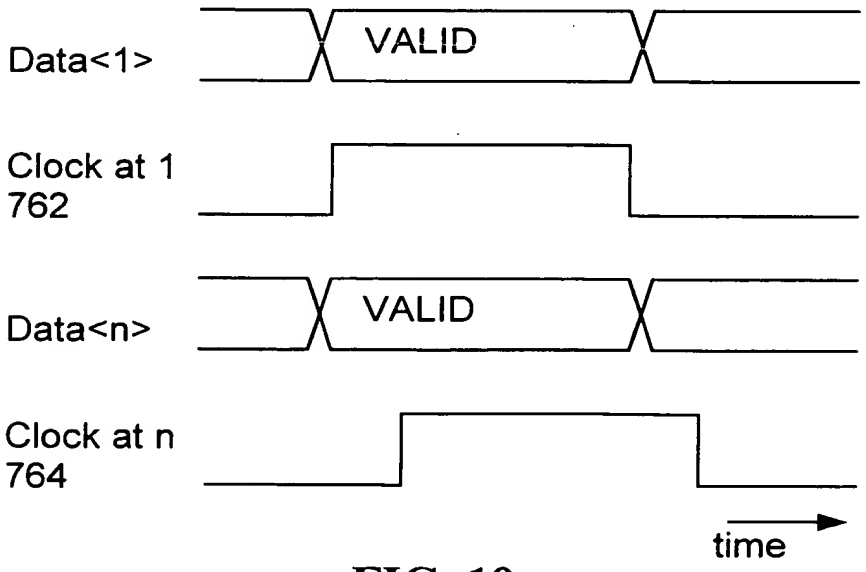

Data<1>
VALID
Clock at 1
762
Data<n>
VALID
Clock at n
764
time

FIG. 19

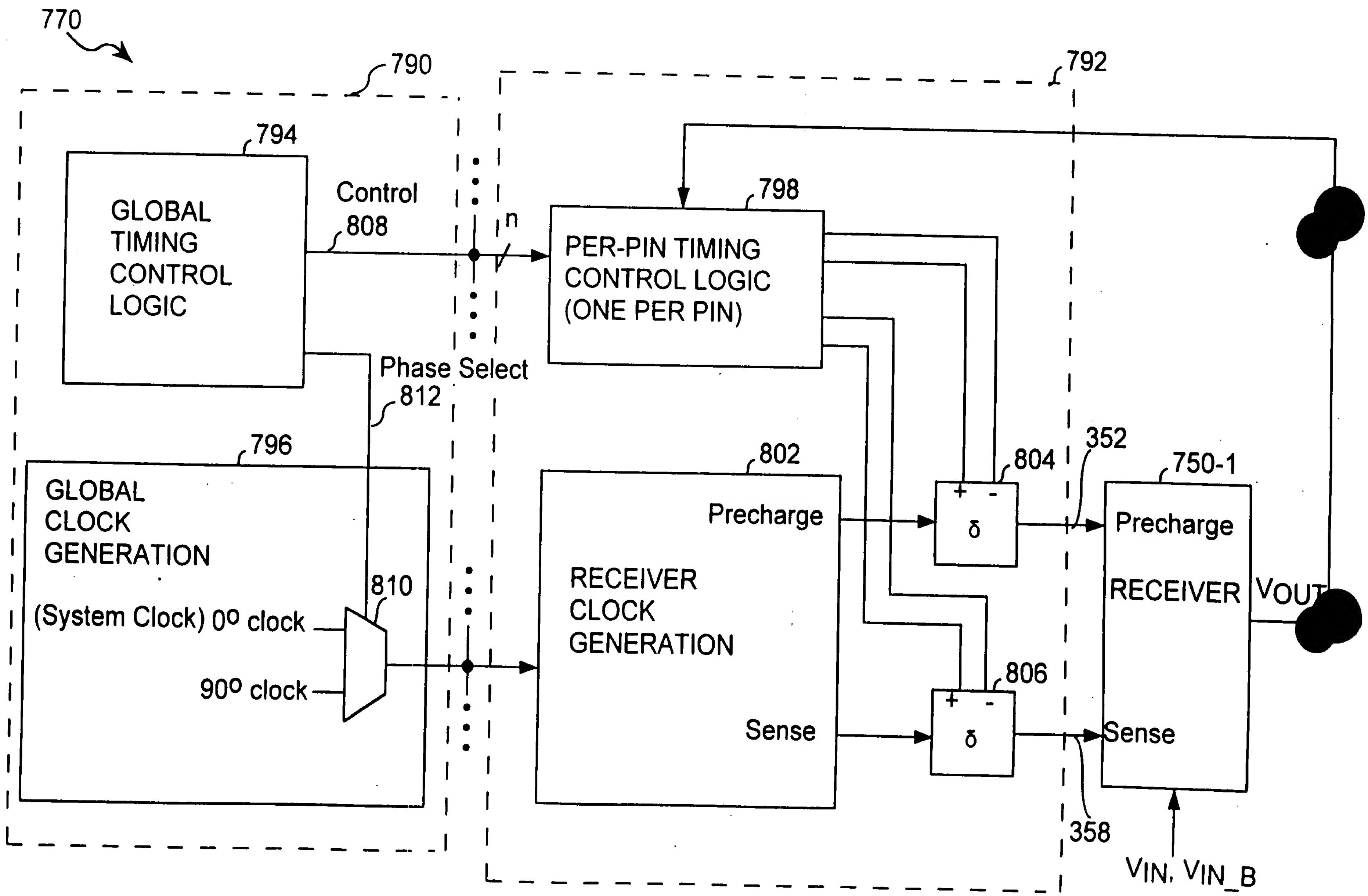

770
790
792
794
GLOBAL TIMING CONTROL LOGIC
Control
808
n
798
PER-PIN TIMING CONTROL LOGIC (ONE PER PIN)
Phase Select
812
796
GLOBAL CLOCK GENERATION
(System Clock) 0o clock
90o clock
810
802
Precharge
RECEIVER CLOCK GENERATION
Sense
804
806
δ
352
358
750-1
Precharge
RECEIVER
Sense
VOUT
VIN, VIN_B

FIG. 20

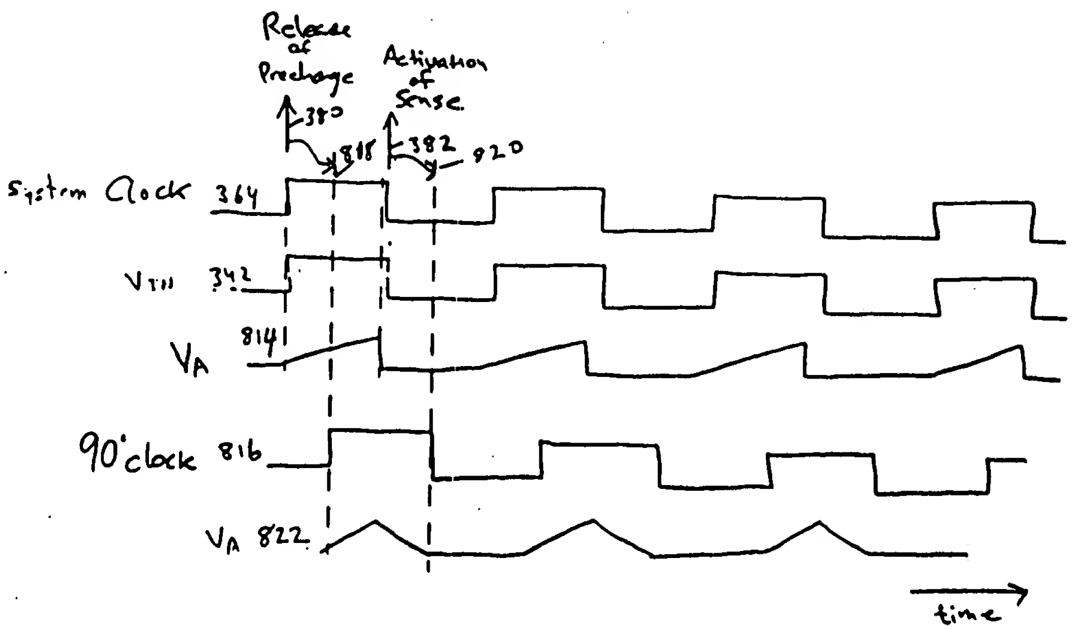

Release of Precharge
380
818
Activation of Sense
382
920
System Clock 364
VTH 342
VA
814
90° clock 816
VA 822
time

FIG. 21

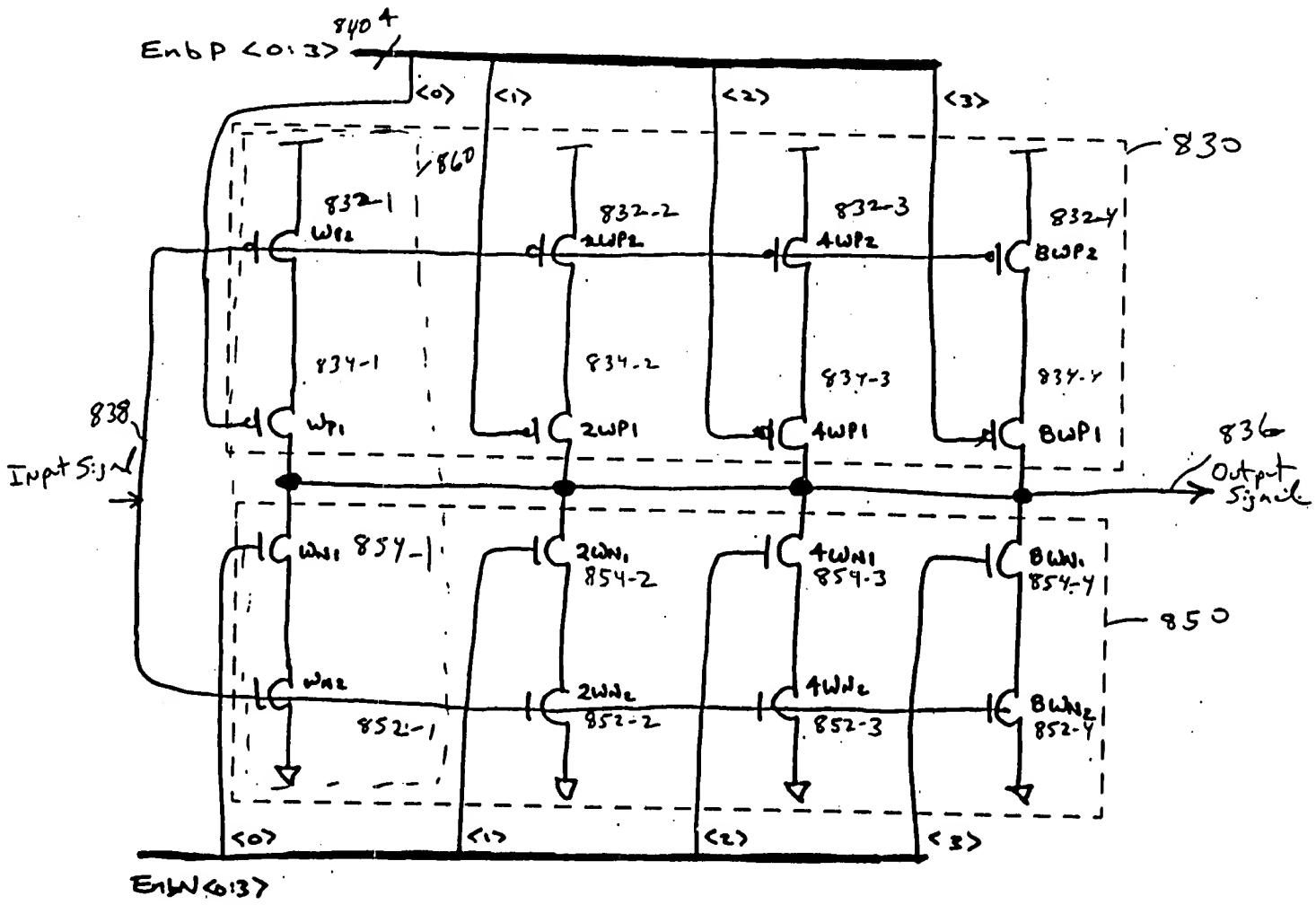


FIG. 22

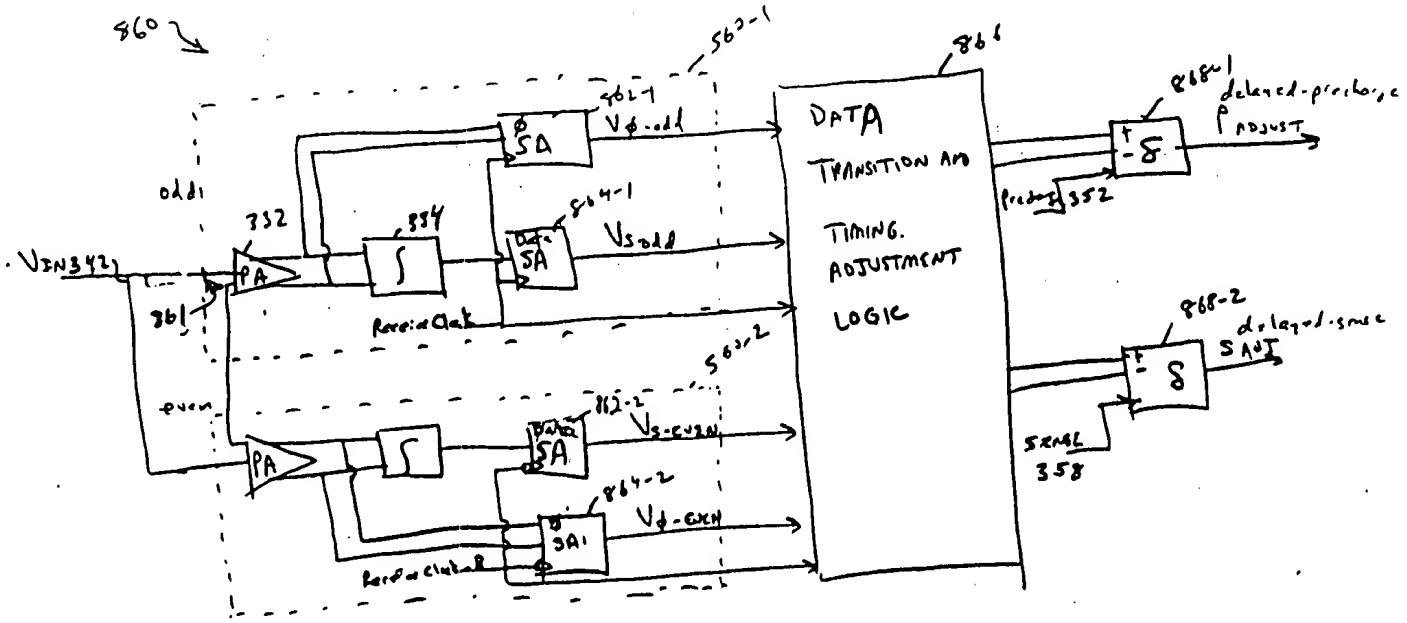


FIG. 23 A

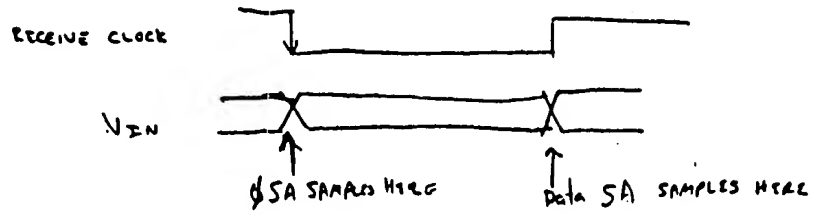


FIG. 23 B

870

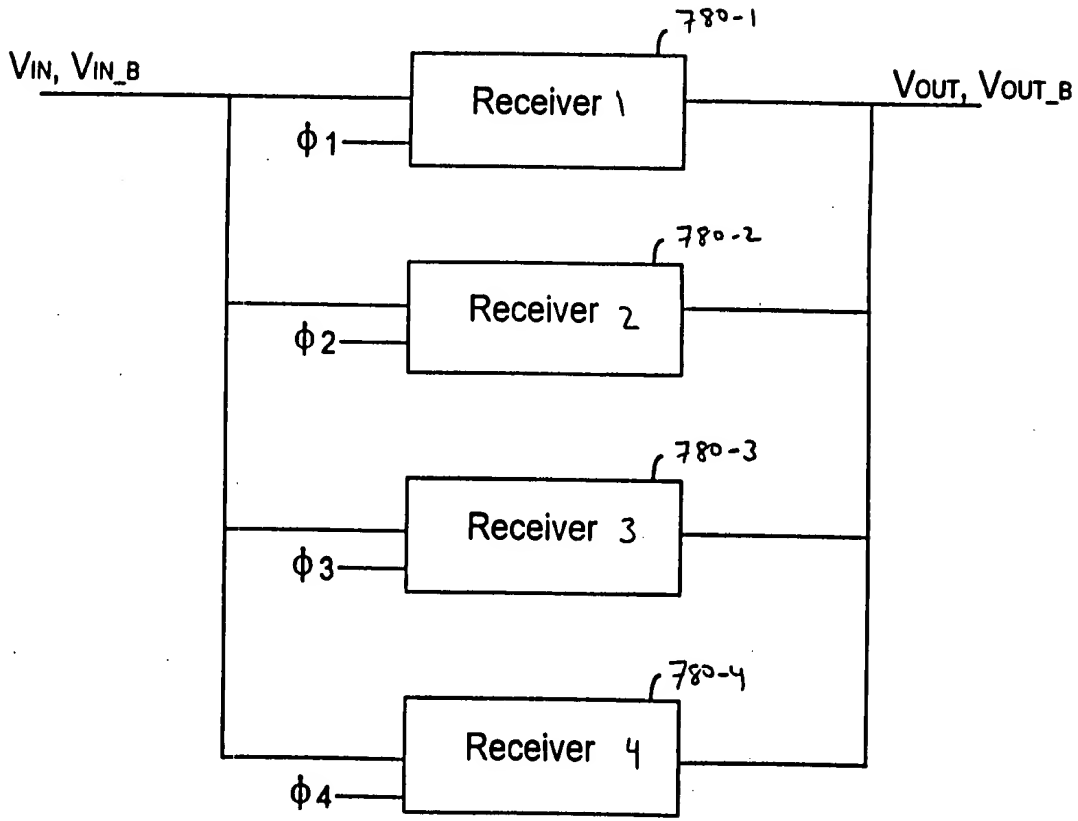


FIG 24

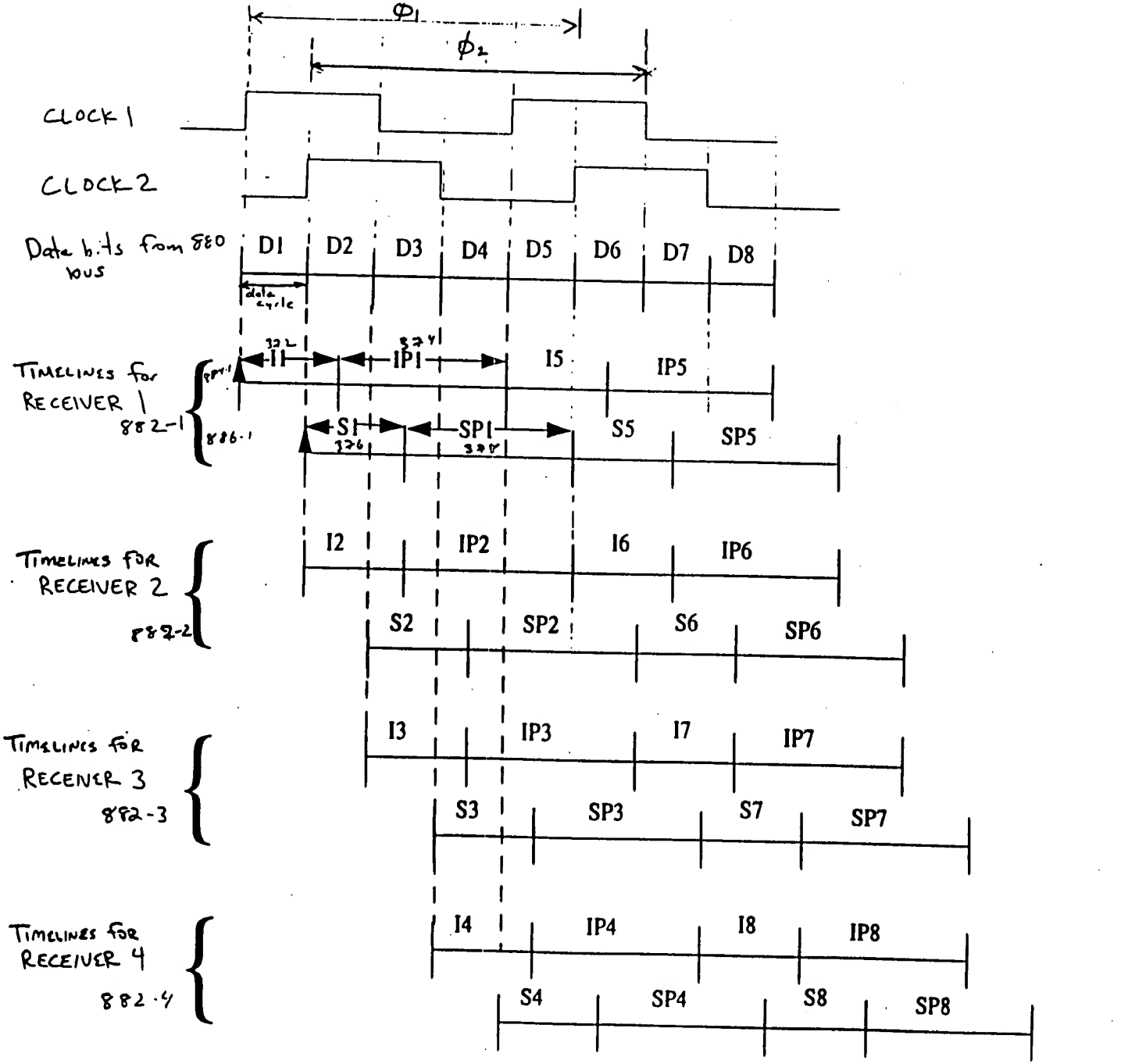


FIG. 25

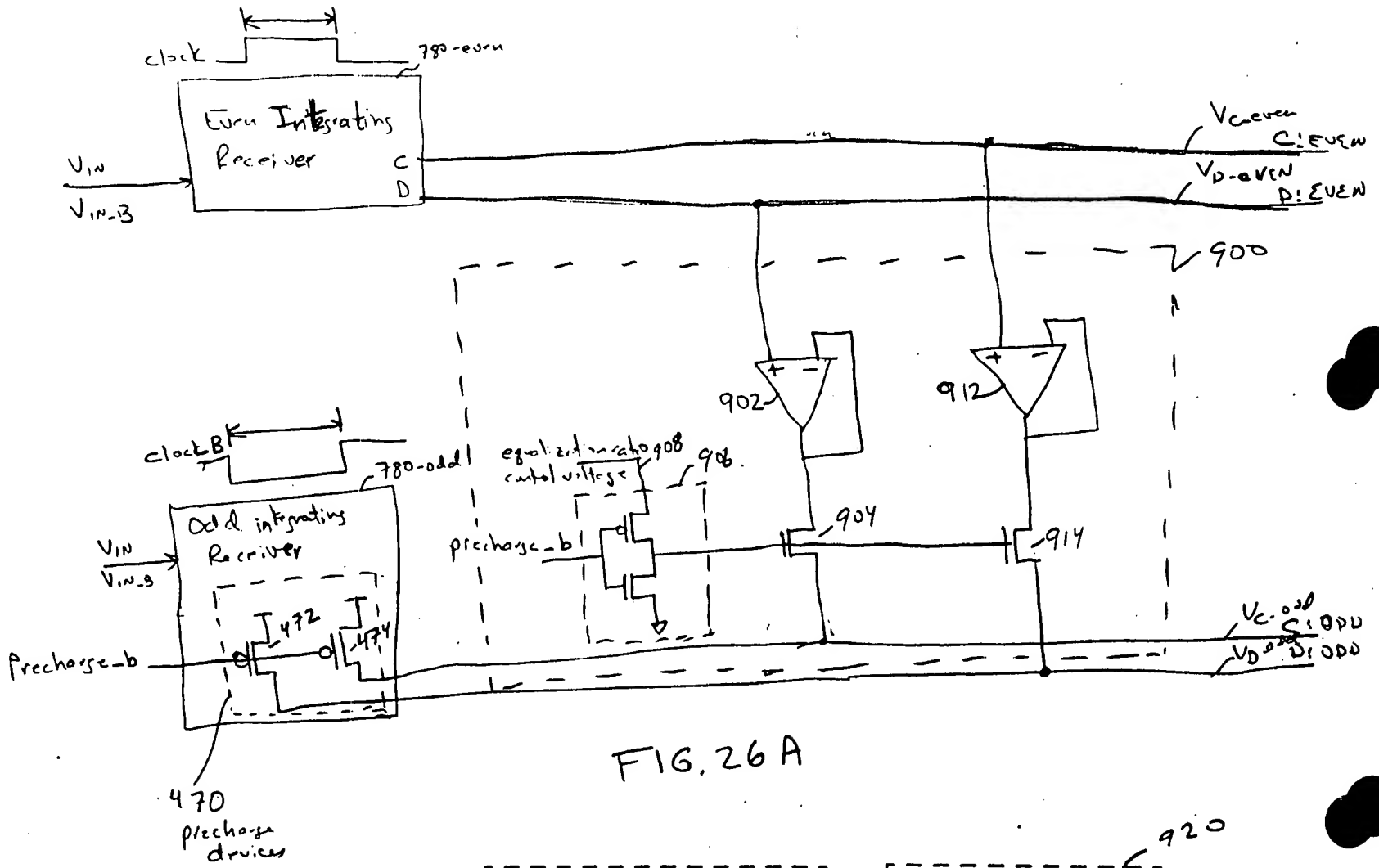


FIG. 26A

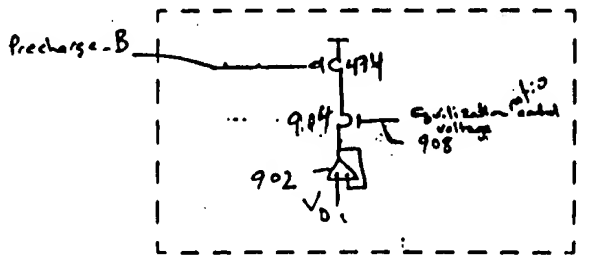


FIG. 26B

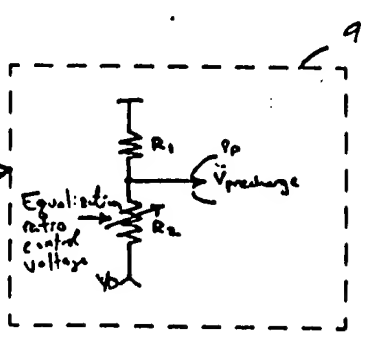


FIG. 26C

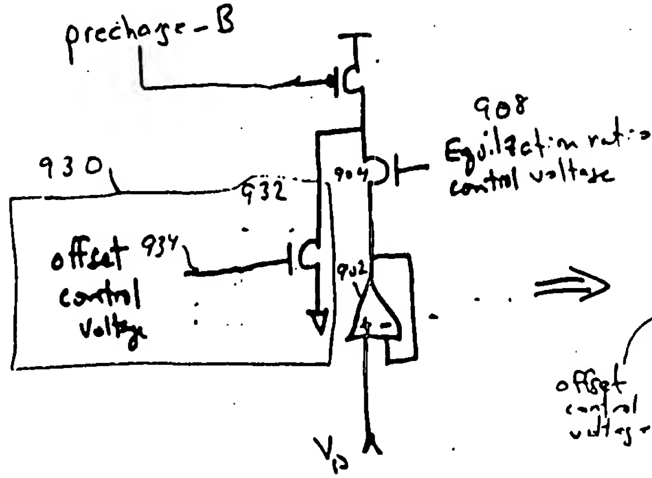


FIG. 27A

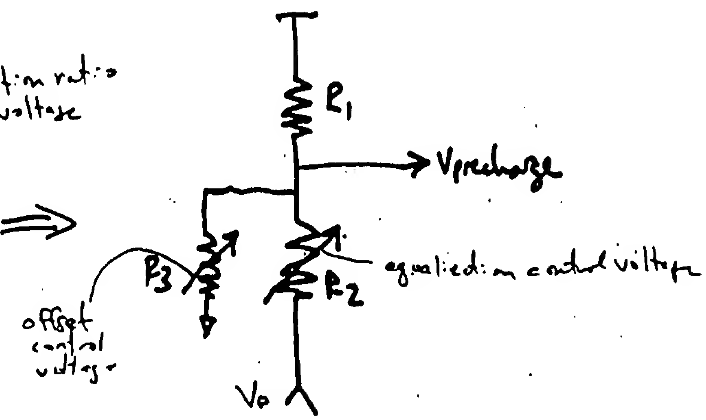


FIG. 27B

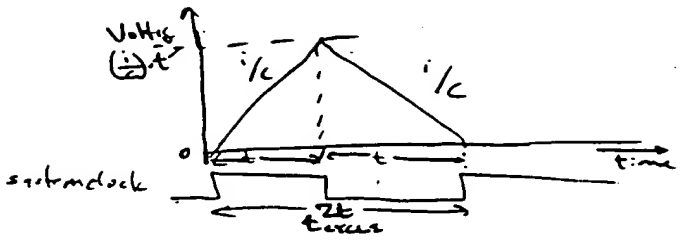


FIG. 28A

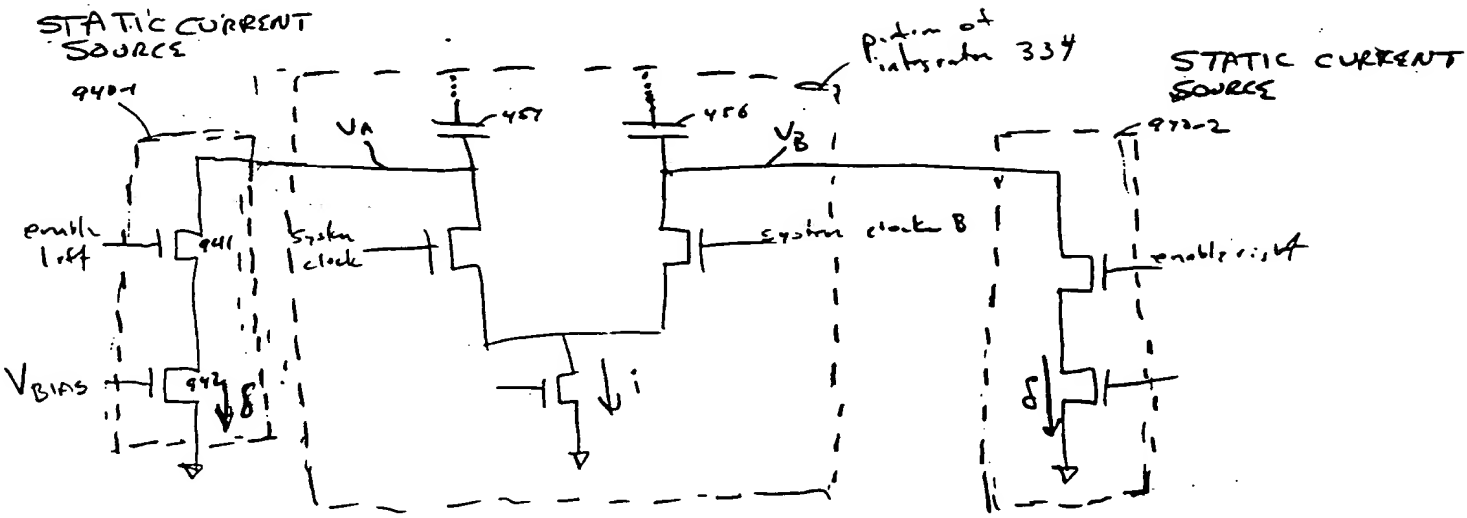


FIG. 28B

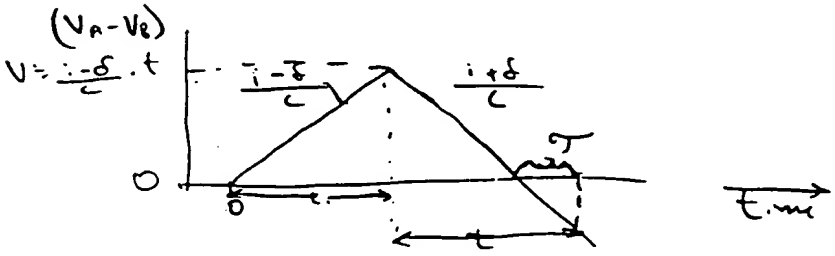


FIG. 28C

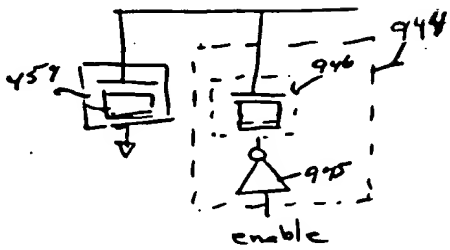


FIG. 28D

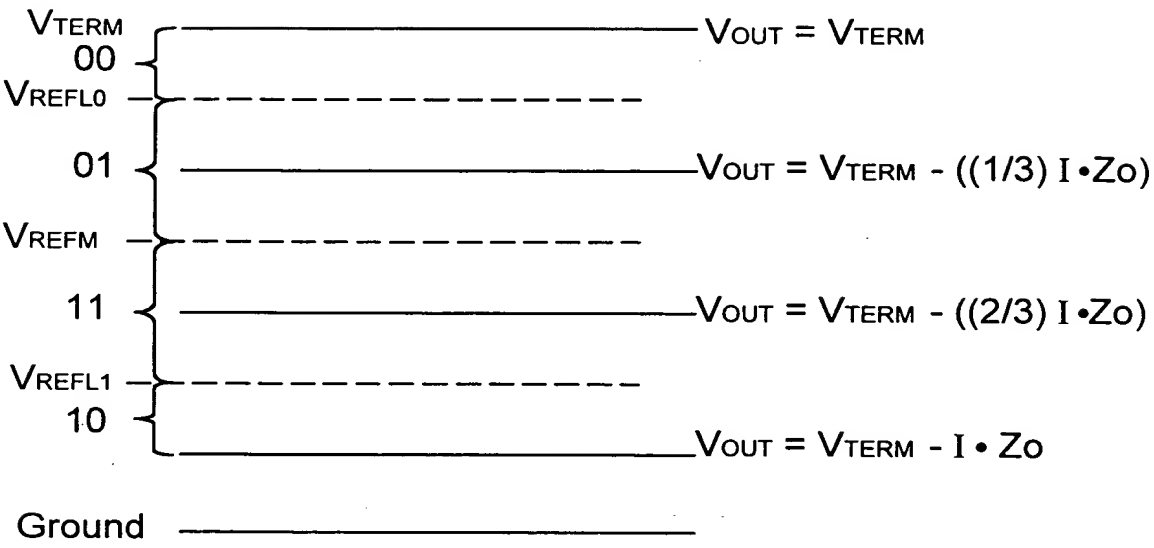

VTERM
00
VREFL0
01
VREFM
11
VREFL1
10
Ground
VOUT = VTERM
VOUT = VTERM - ((1/3) I •Zo)
VOUT = VTERM - ((2/3) I •Zo)
VOUT = VTERM - I • Zo

FIG. 29

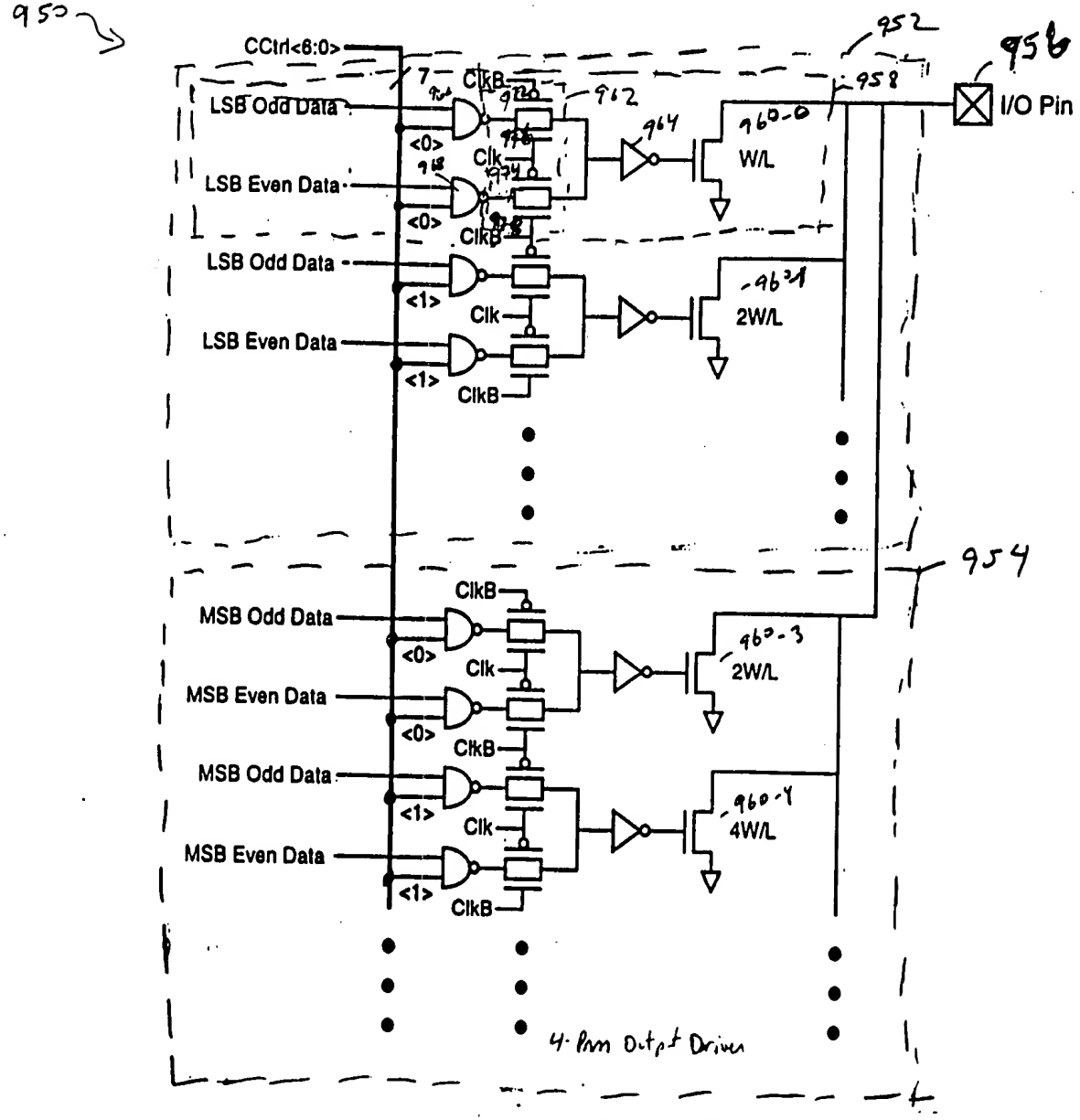


FIG. 30

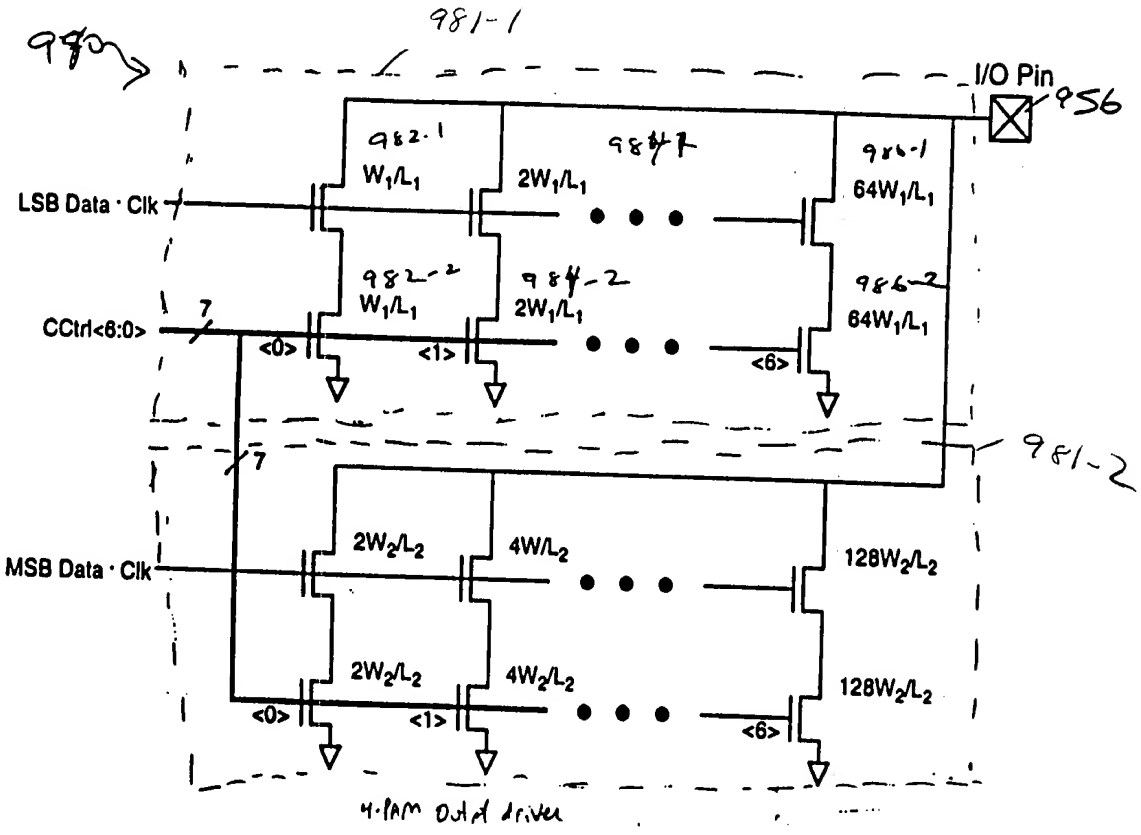


FIG. 31

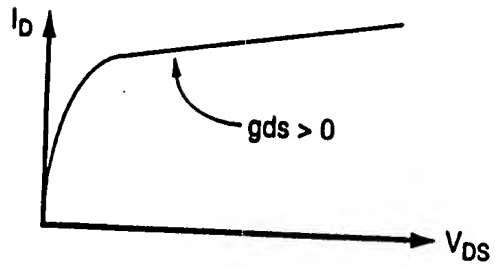


FIG. 32A

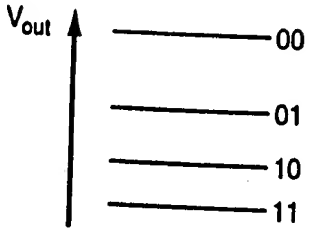


FIG. 32B

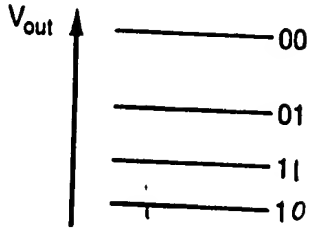


FIG. 32C

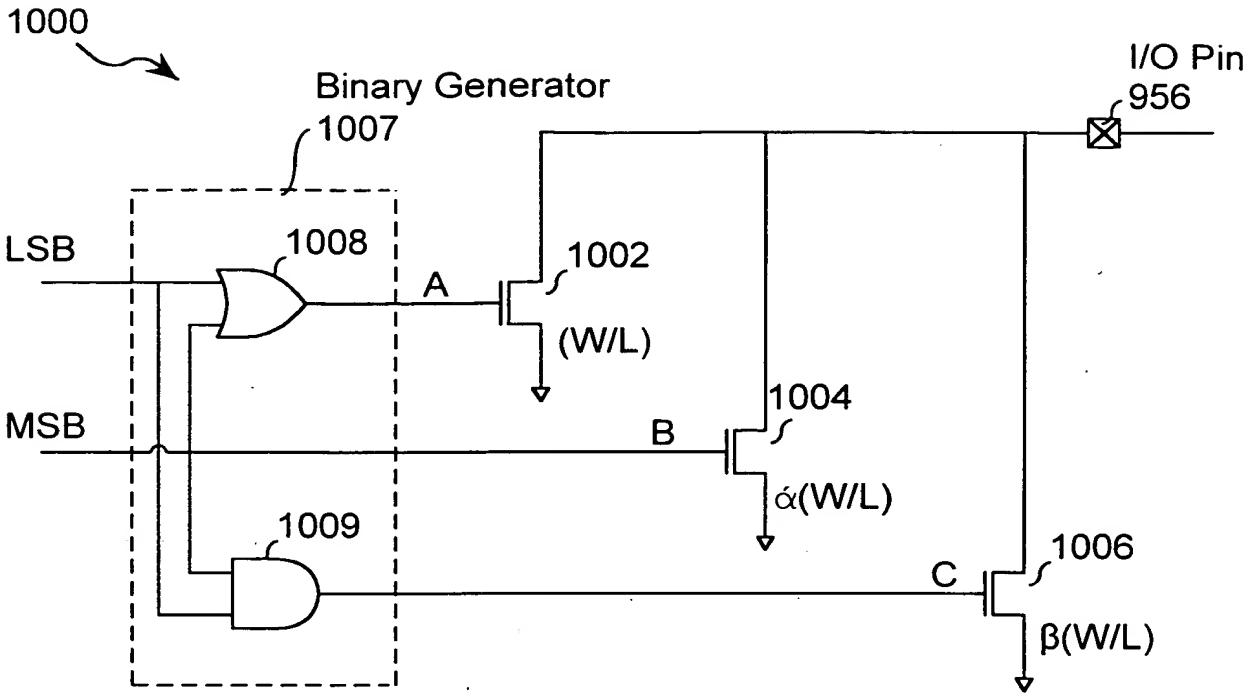
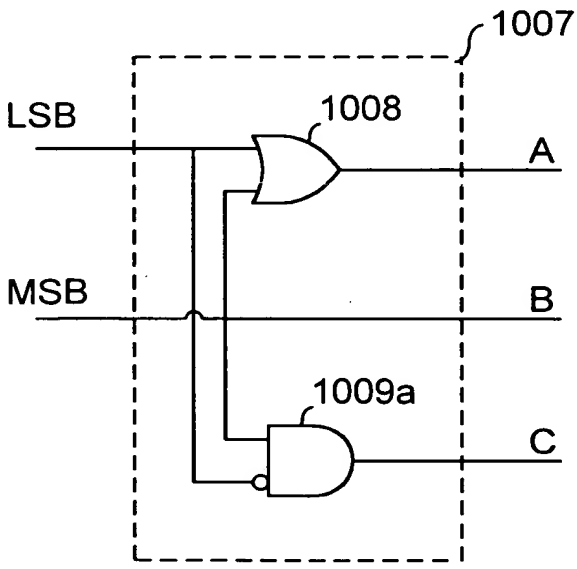
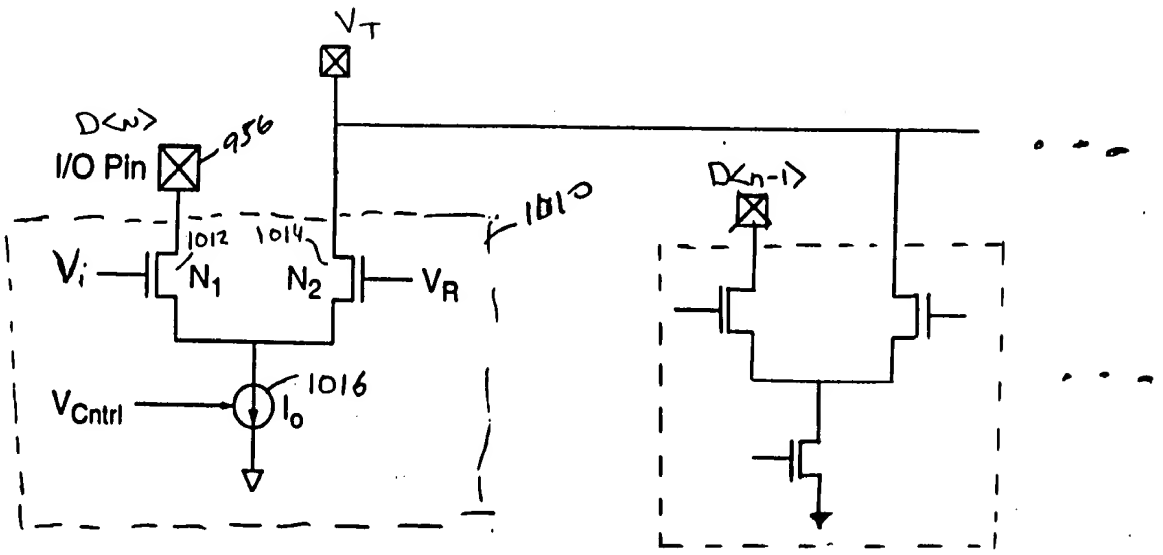


FIG. 33A



Gray Code Generator

FIG. 33B



circuit to Reduce Switching Noise

FIG. 34.

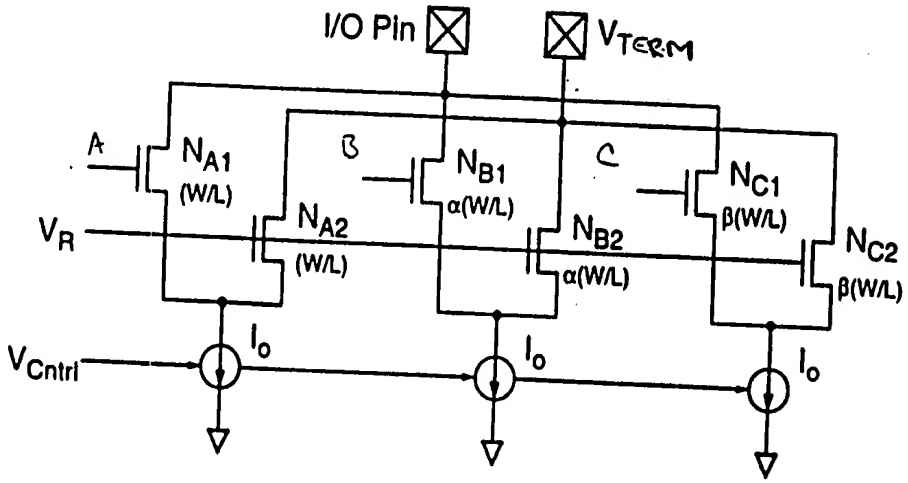
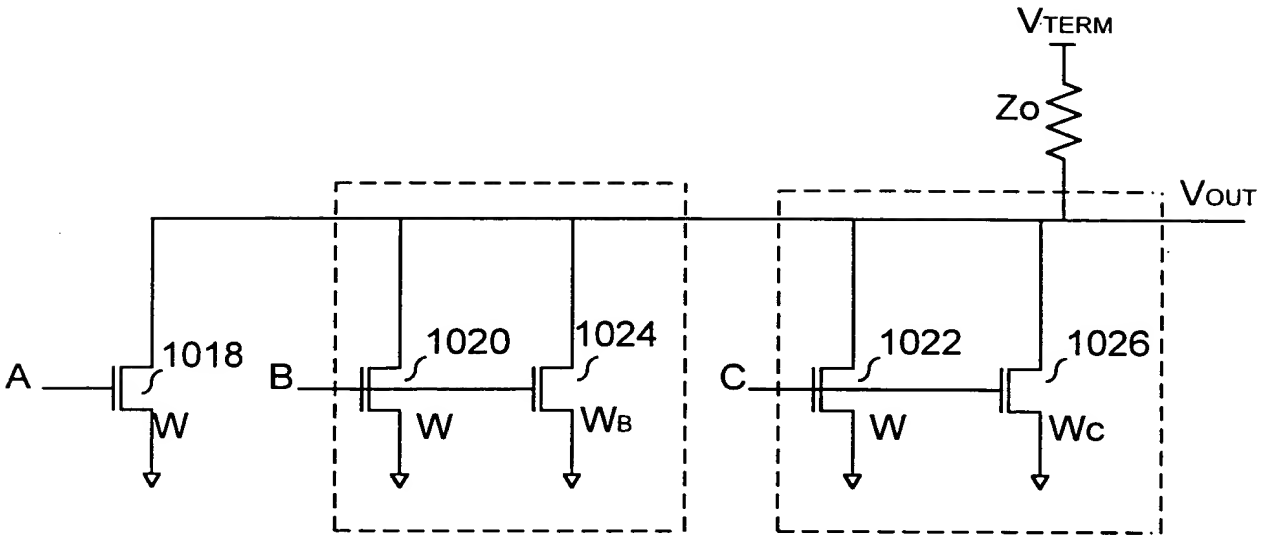
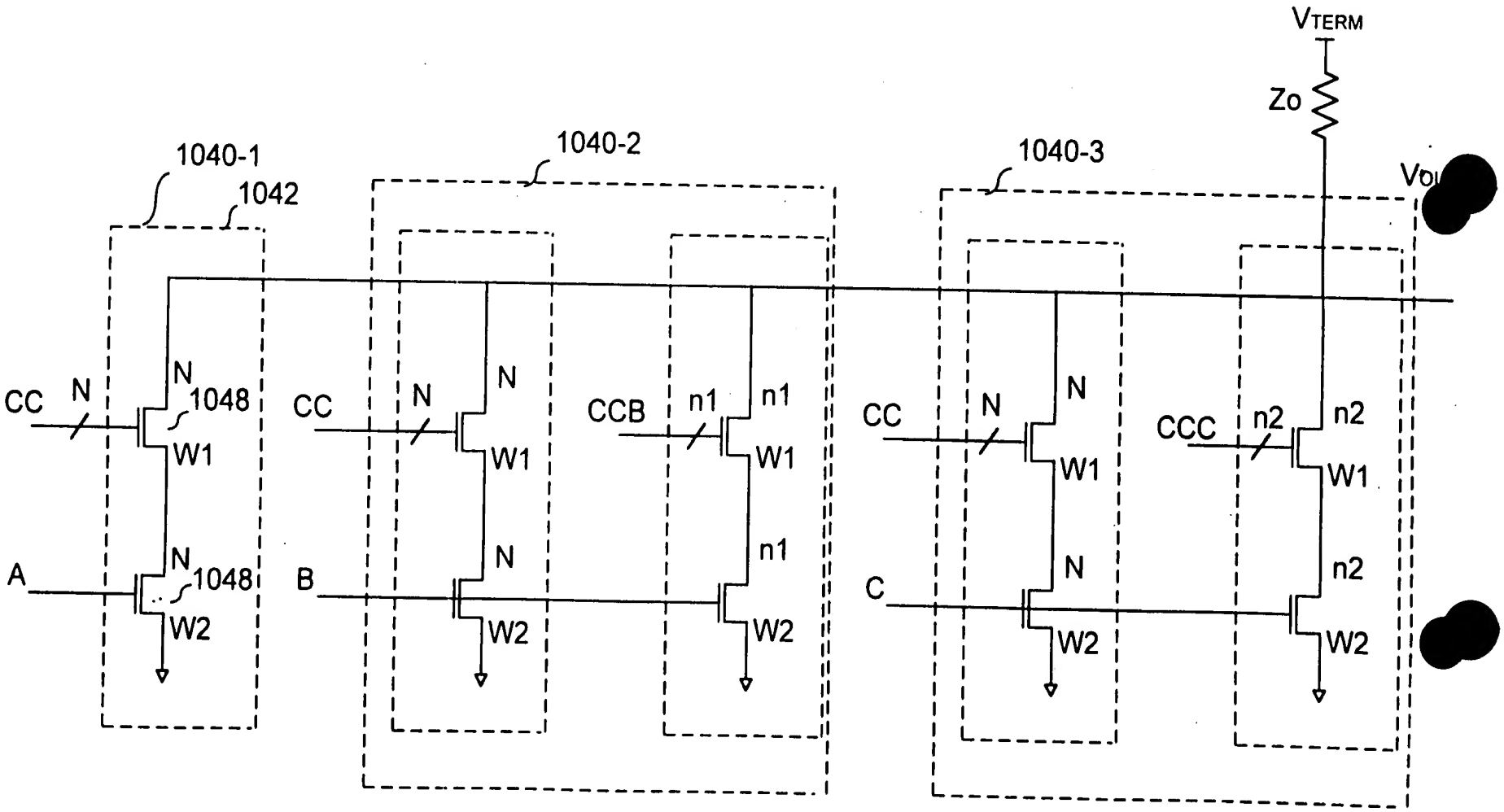


FIG. 35



GDS Compensated Multi-PAM Output Driver

FIG. 36



GDS Compensated Multi-PAM Output Driver with Current Control

FIG. 37A

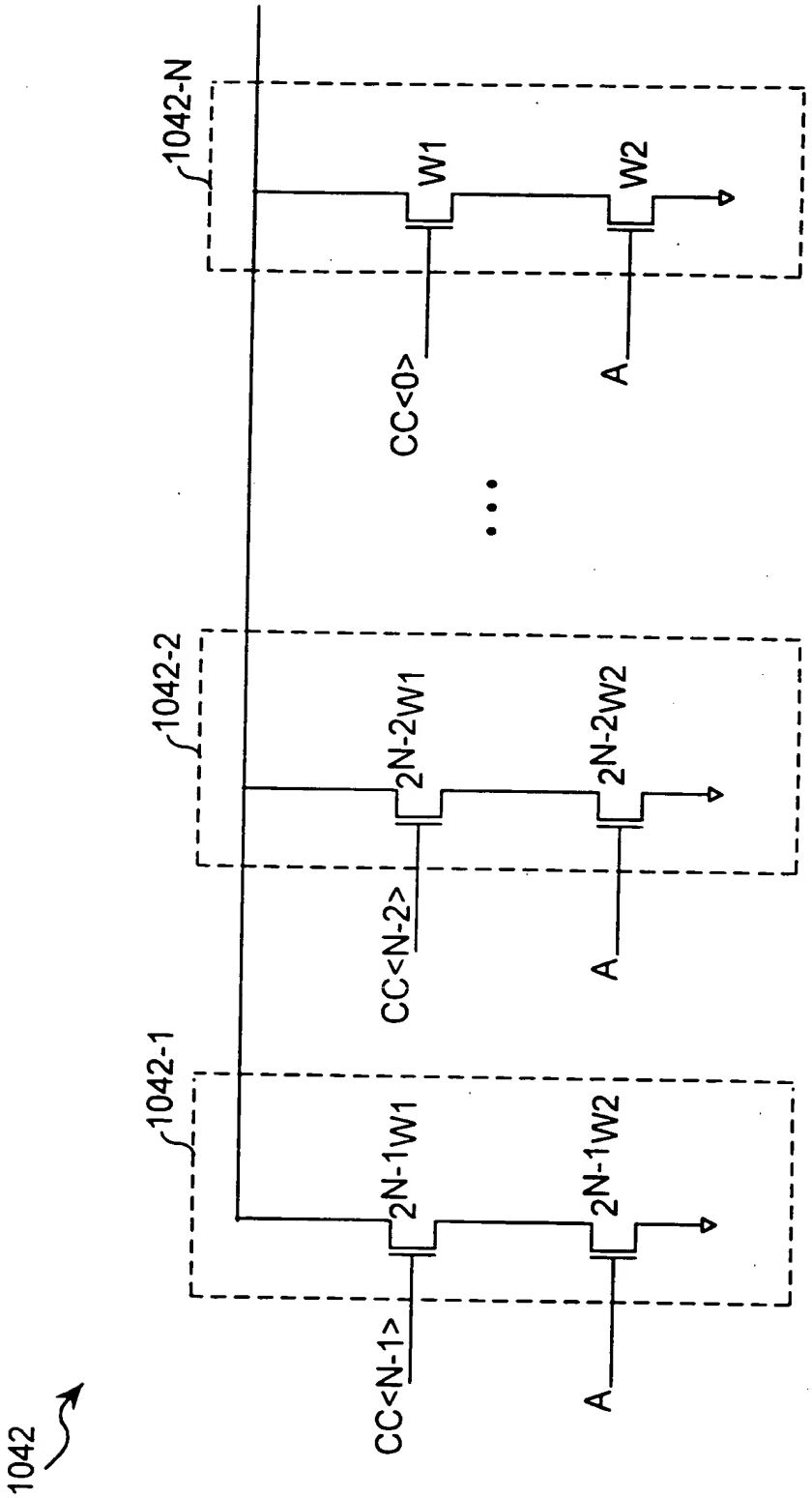
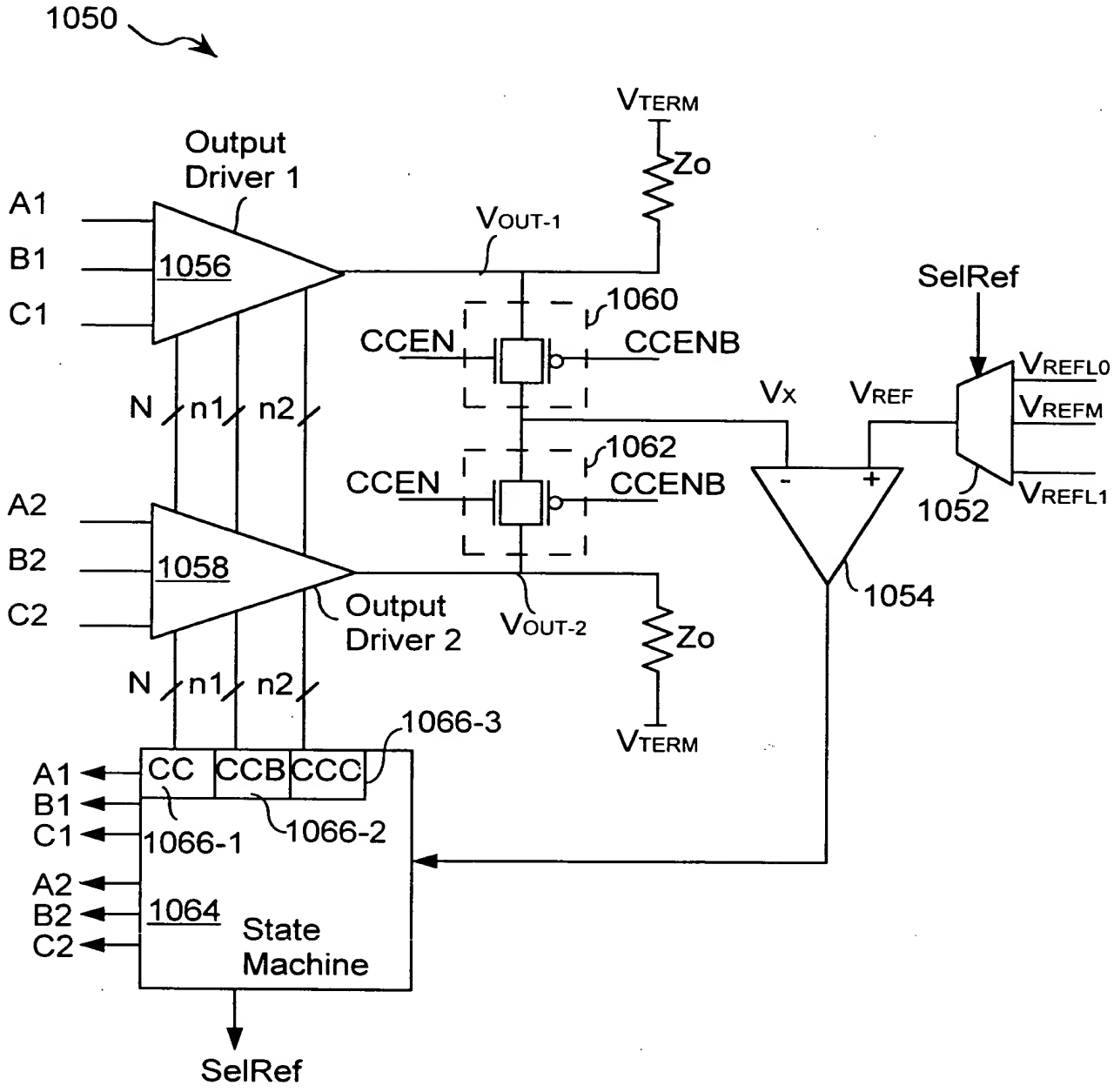
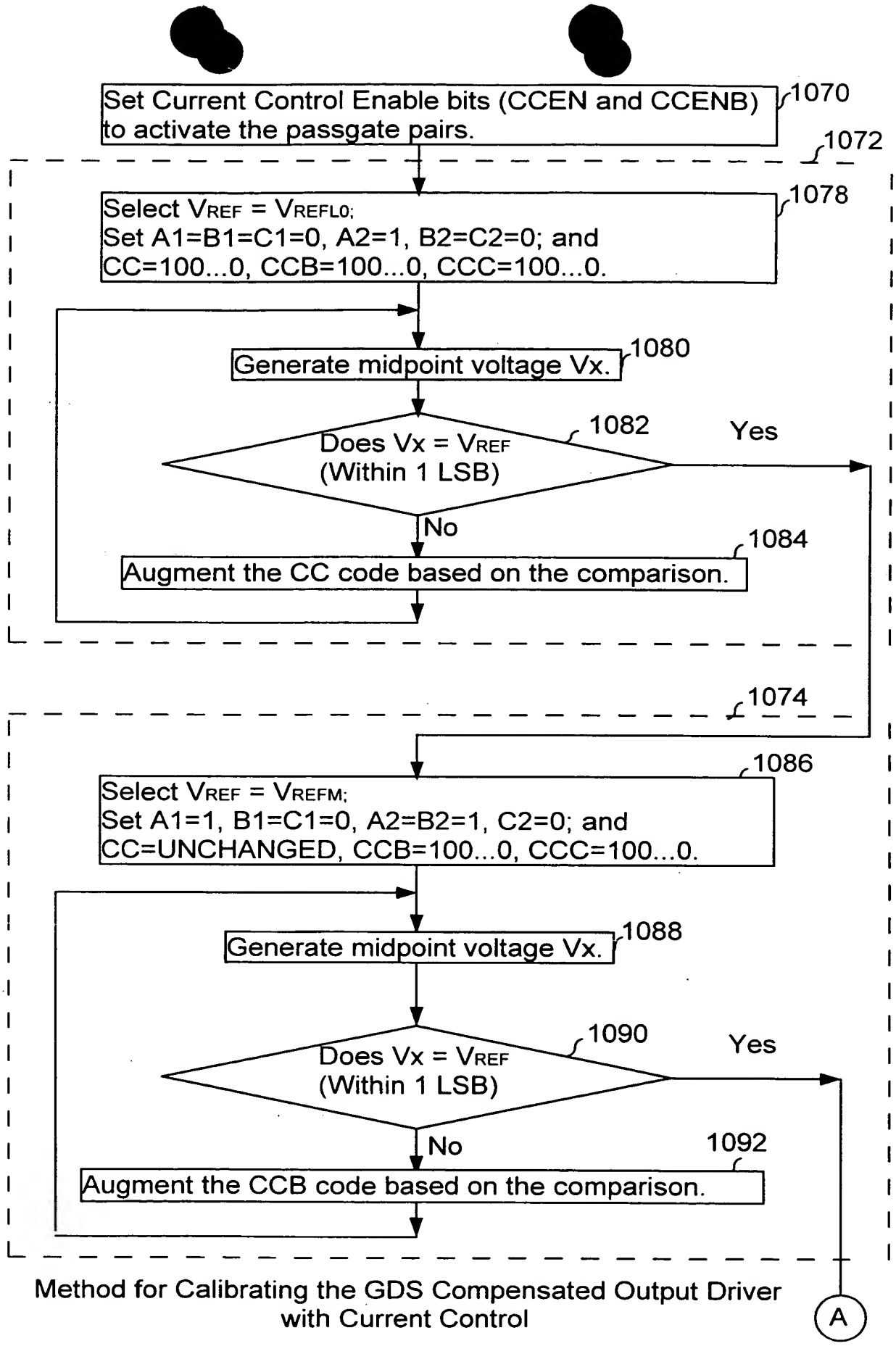

1042
1042-1
1042-2
1042-N
2N-1W1
2N-1W2
2N-2W1
2N-2W2
W1
W2
CC<N-1>
CC<N-2>
CC<0>
A
A
A

FIG. 37B



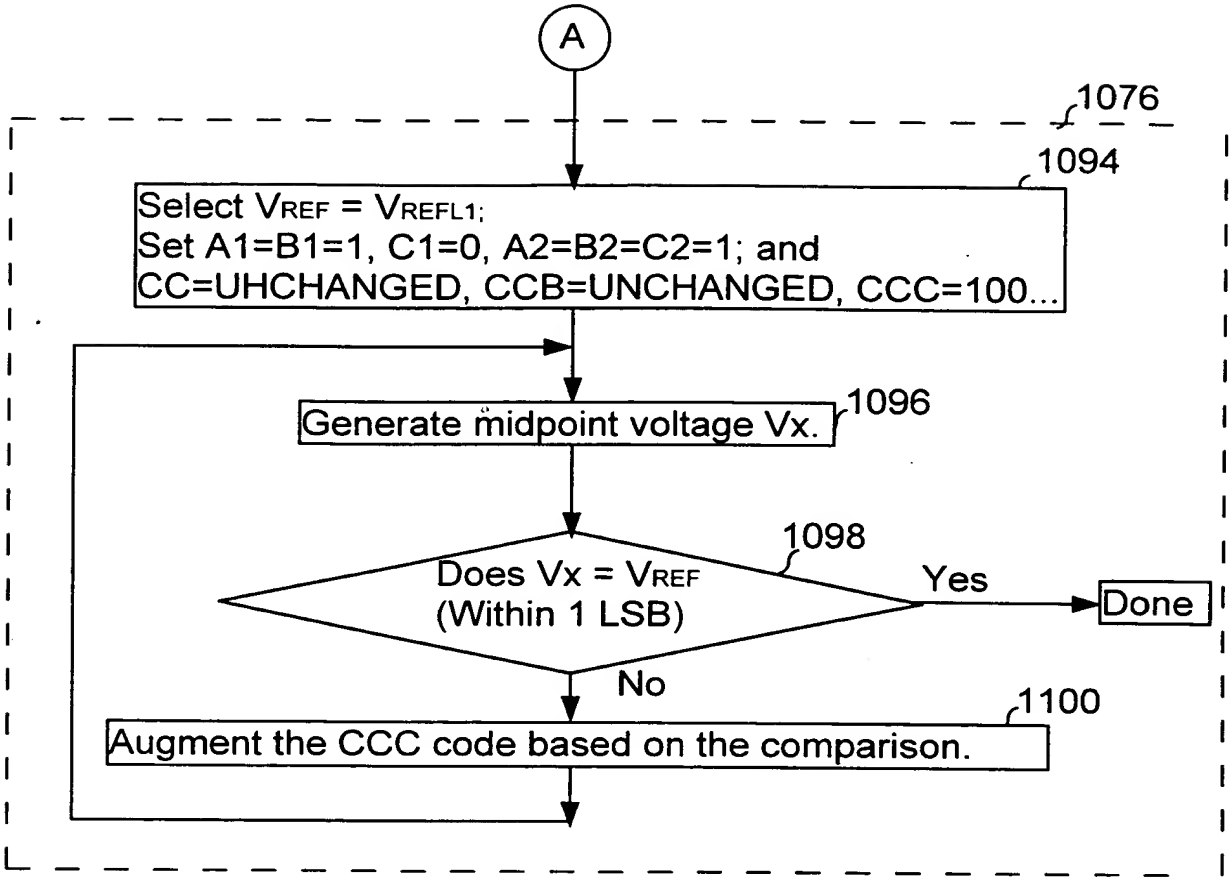
Circuit for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 38



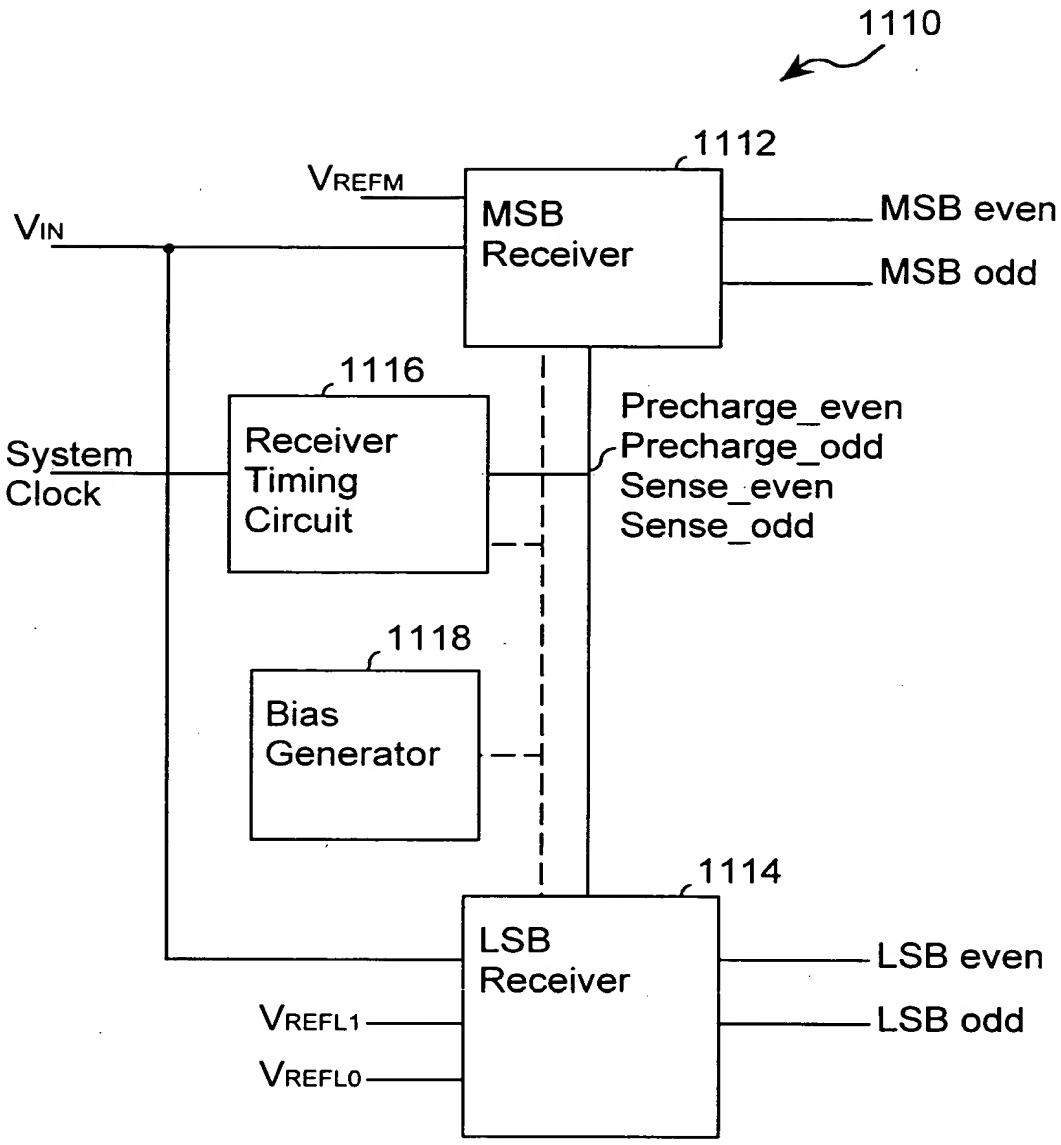
Method for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 39A



Method for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 39B



Multi-PAM Receiver

FIG. 40

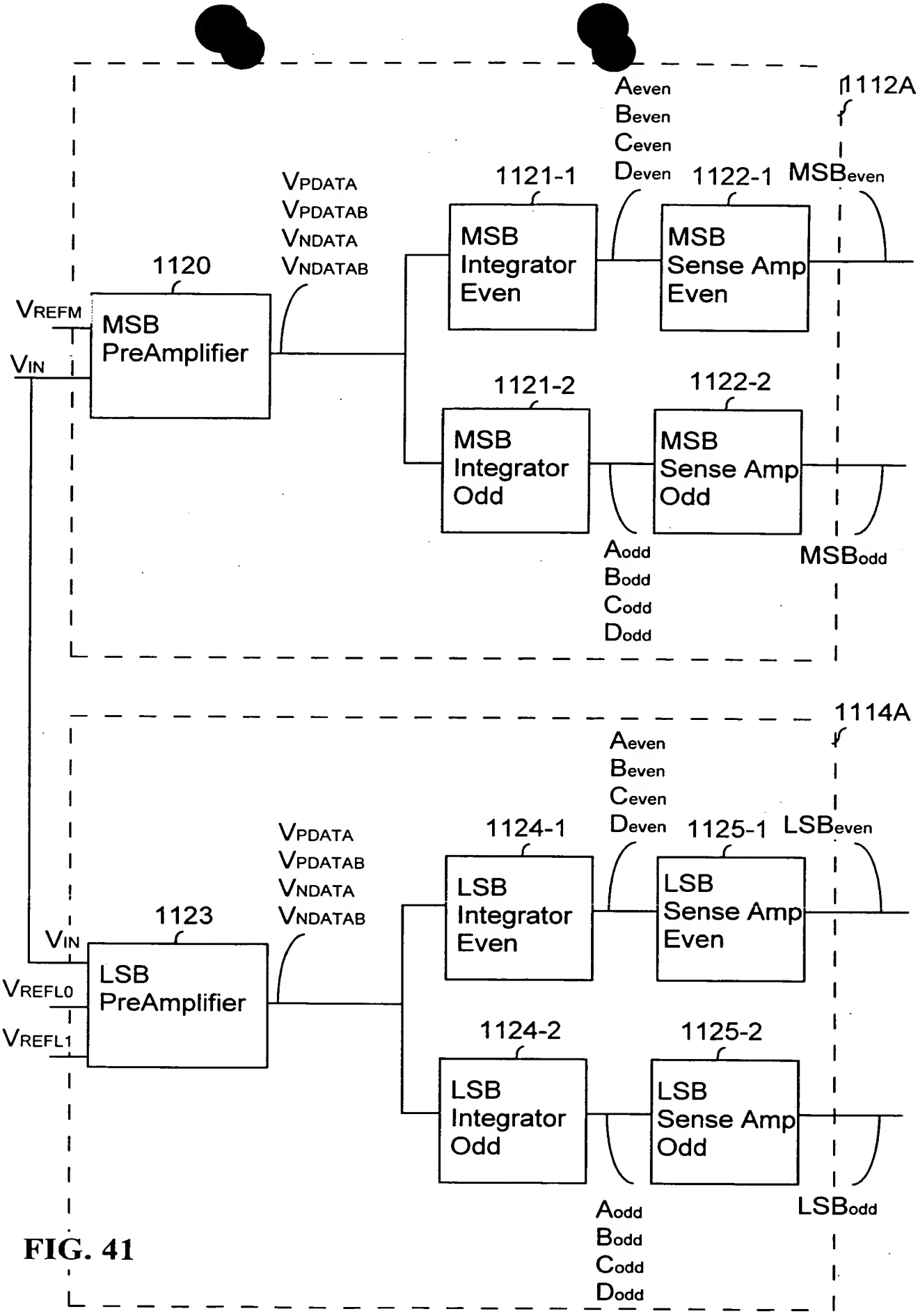

1112A
Aeven
Beven
Ceven
Deven
1121-1
1122-1
MSBeven
VPDATA
VPDATAB
VNDATA
VNDATAB
1120
VREFM
MSB
PreAmplifier
VIN
MSB
Integrator
Even
MSB
Sense Amp
Even
1121-2
1122-2
MSB
Integrator
Odd
MSB
Sense Amp
Odd
Aodd
Bodd
Codd
Dodd
MSBodd
1114A
Aeven
Beven
Ceven
Deven
1124-1
1125-1
LSBeven
VPDATA
VPDATAB
VNDATA
VNDATAB
1123
VIN
LSB
PreAmplifier
VREFL0
VREFL1
LSB
Integrator
Even
LSB
Sense Amp
Even
1124-2
1125-2
LSB
Integrator
Odd
LSB
Sense Amp
Odd
Aodd
Bodd
Codd
Dodd
LSBodd

FIG. 41

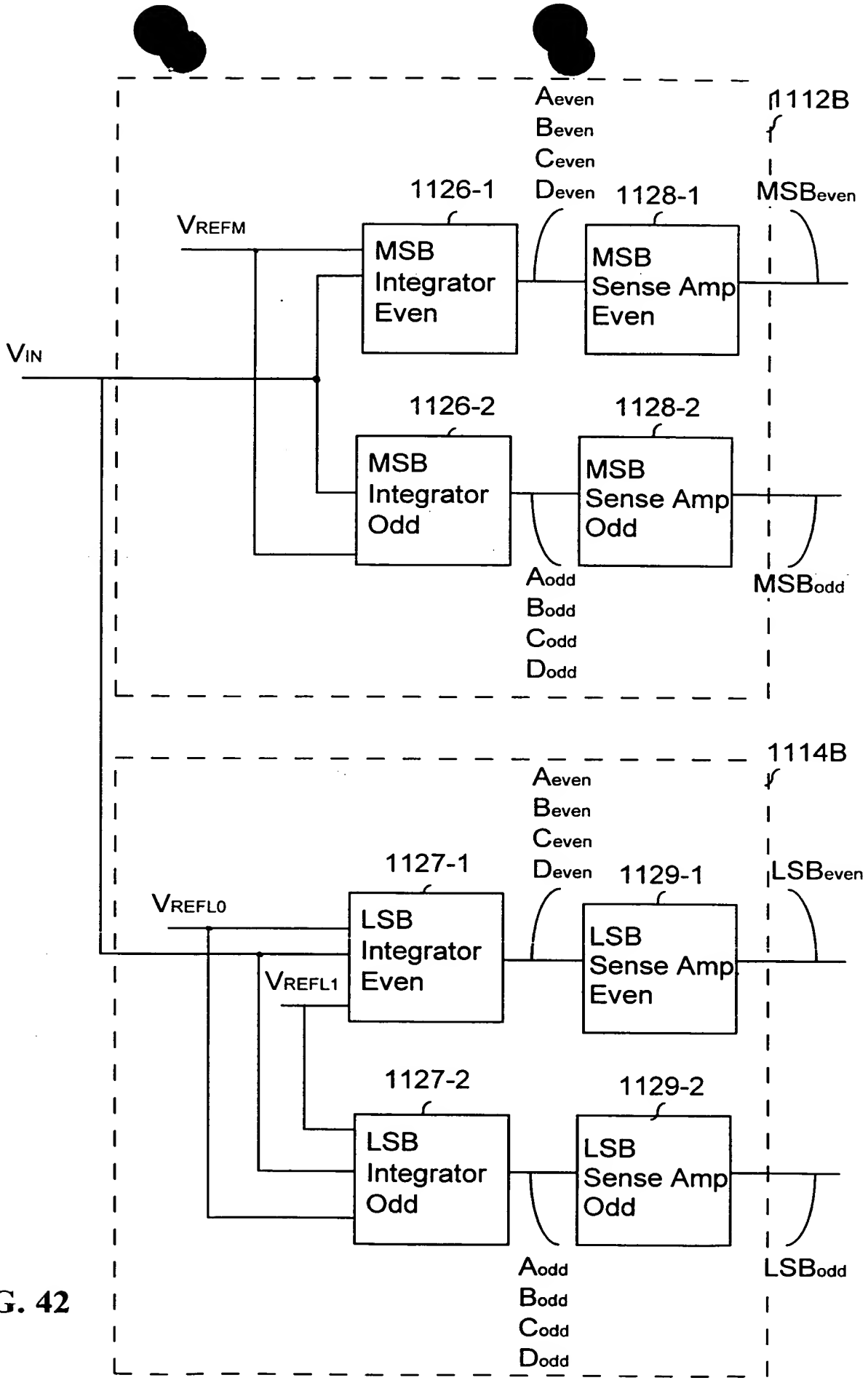
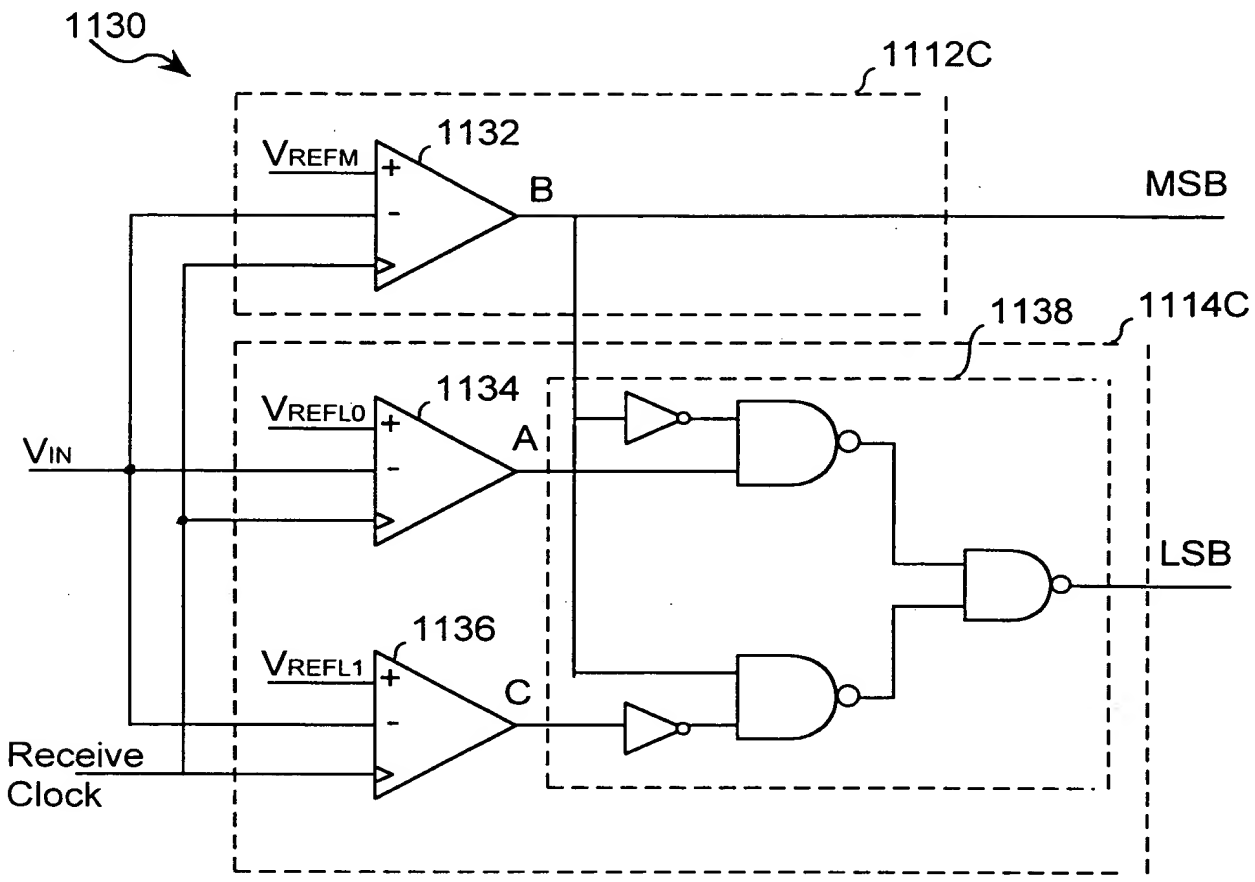
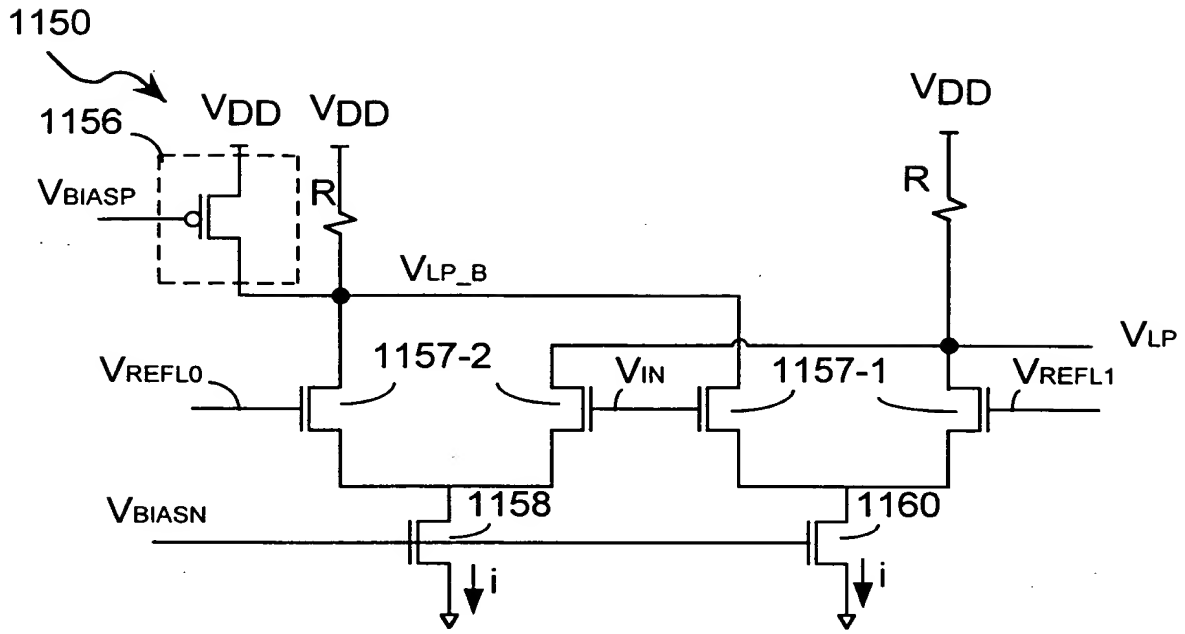

1112B
Aeven
Beven
Ceven
Deven
1126-1
1128-1
MSBeven
VREFM
MSB Integrator Even
MSB Sense Amp Even
VIN
1126-2
1128-2
MSB Integrator Odd
MSB Sense Amp Odd
Aodd
Bodd
Codd
Dodd
MSBodd
1114B
Aeven
Beven
Ceven
Deven
1127-1
1129-1
LSBeven
VREFL0
LSB Integrator Even
LSB Sense Amp Even
VREFL1
1127-2
1129-2
LSB Integrator Odd
LSB Sense Amp Odd
Aodd
Bodd
Codd
Dodd
LSBodd

FIG. 42



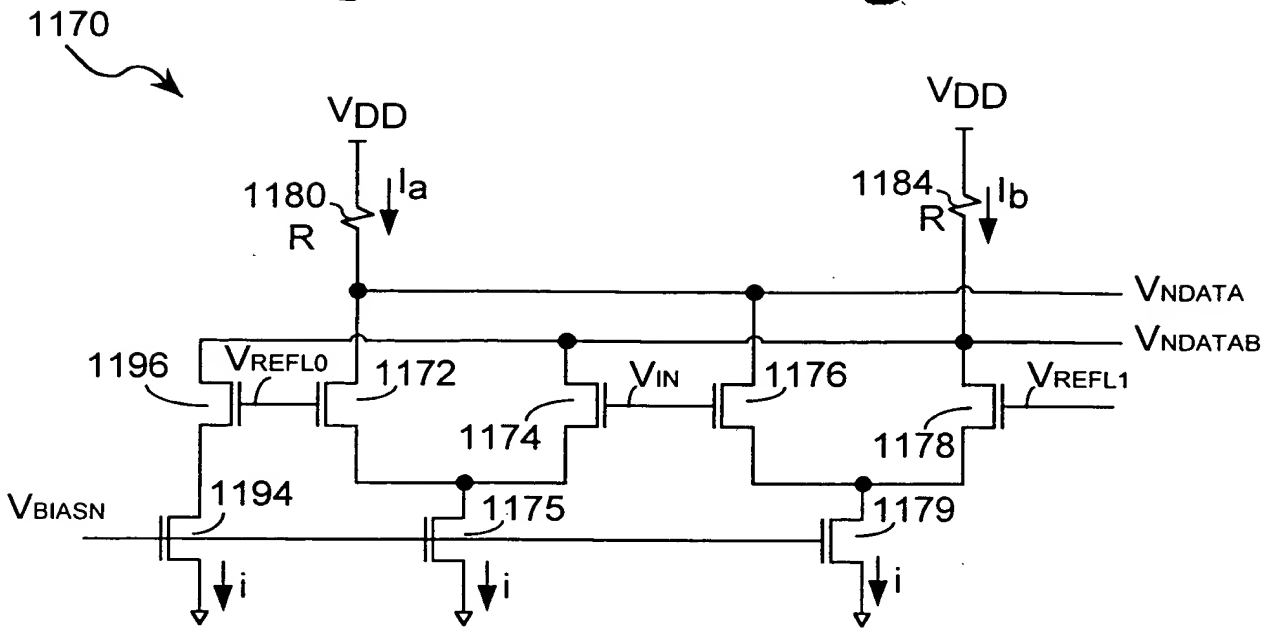
Multi-PAM Receiver

FIG. 43



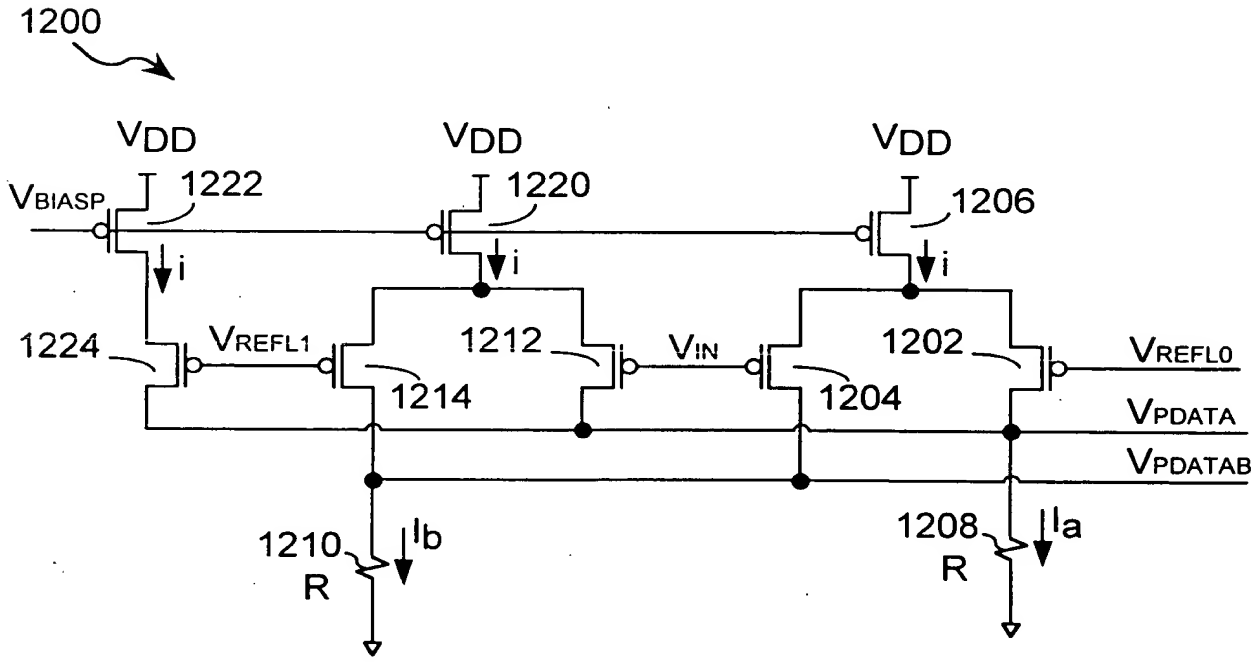
Multi-PAM Pre-Amplifier

FIG. 44



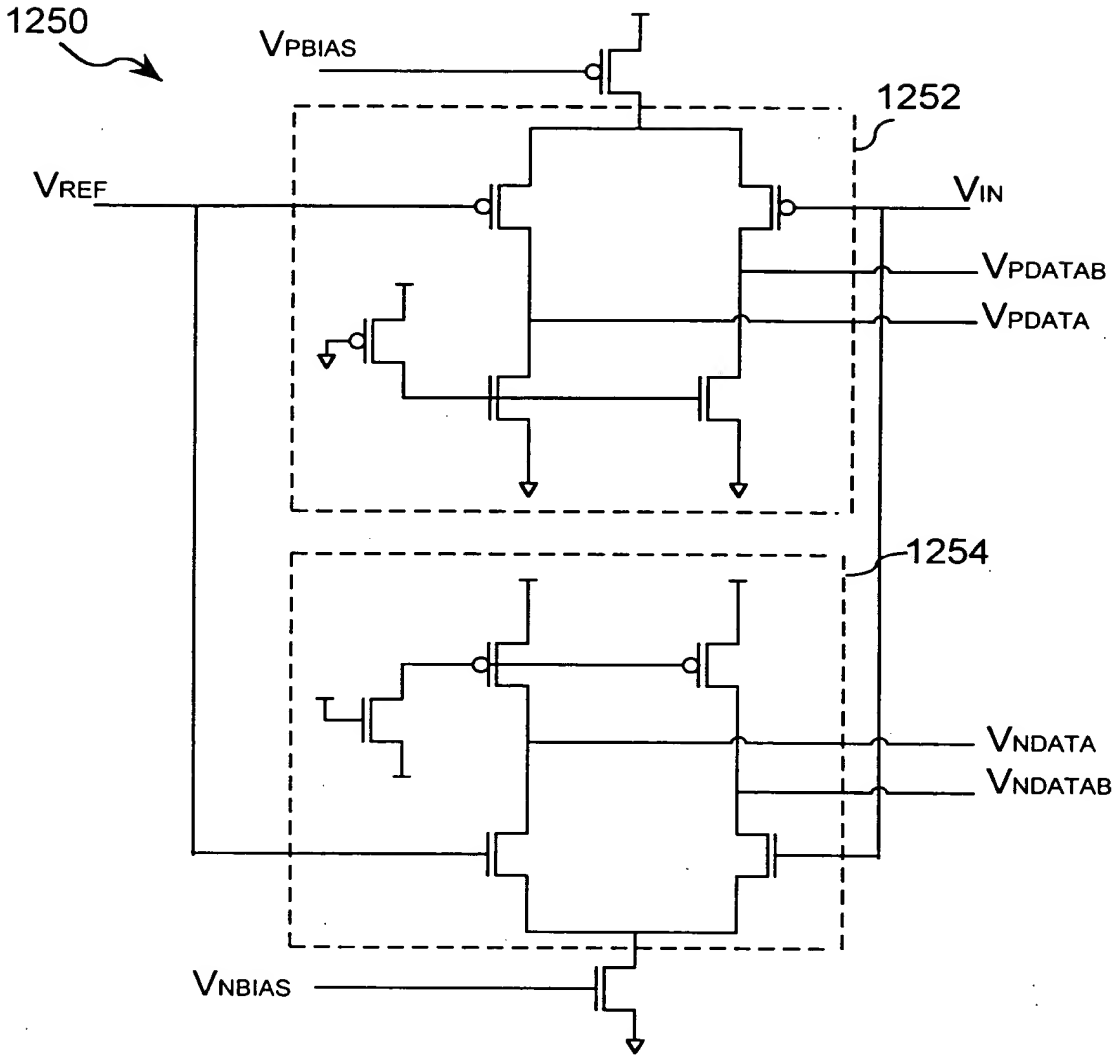
Multi-PAM Pre-Amplifier

FIG. 45A



Multi-PAM Pre-Amplifier

FIG. 45B



Multi-PAM Pre-Amplifier for MSB

FIG. 46

LSB FOLDED INTEGRATOR

1330

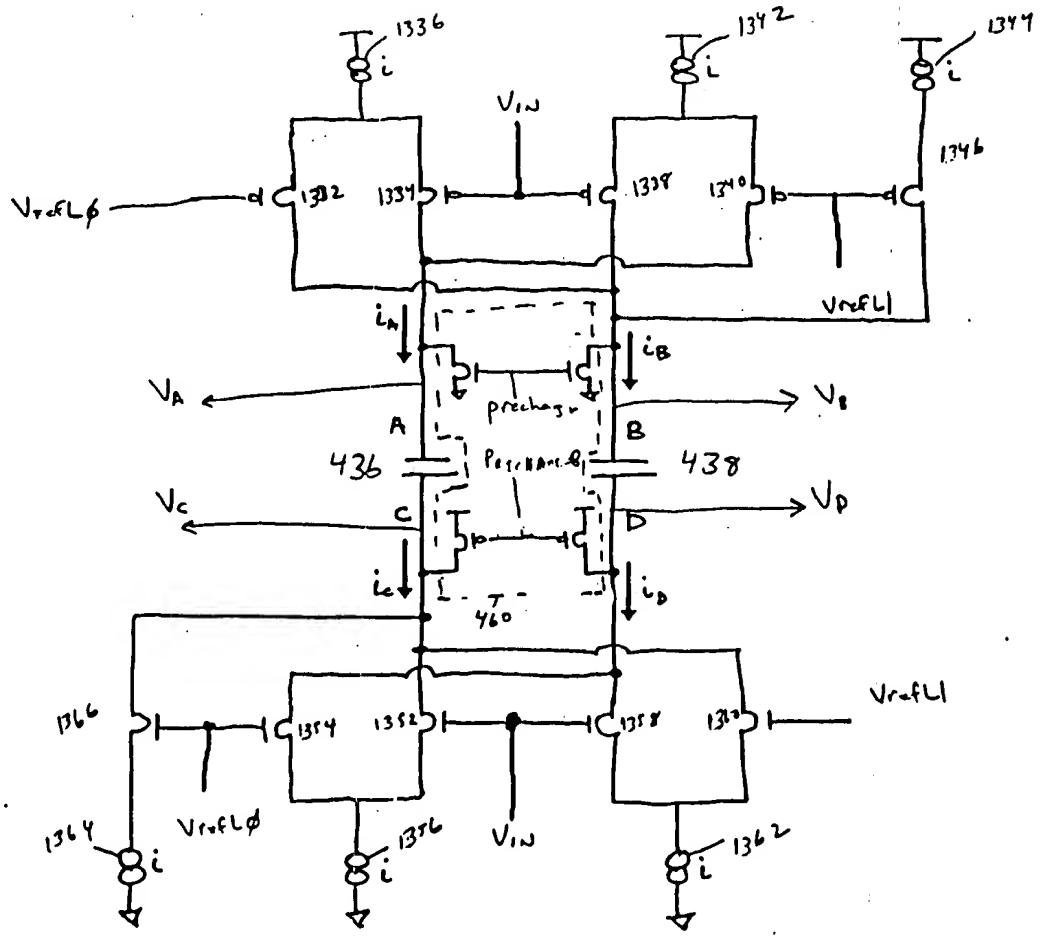


FIG. 47

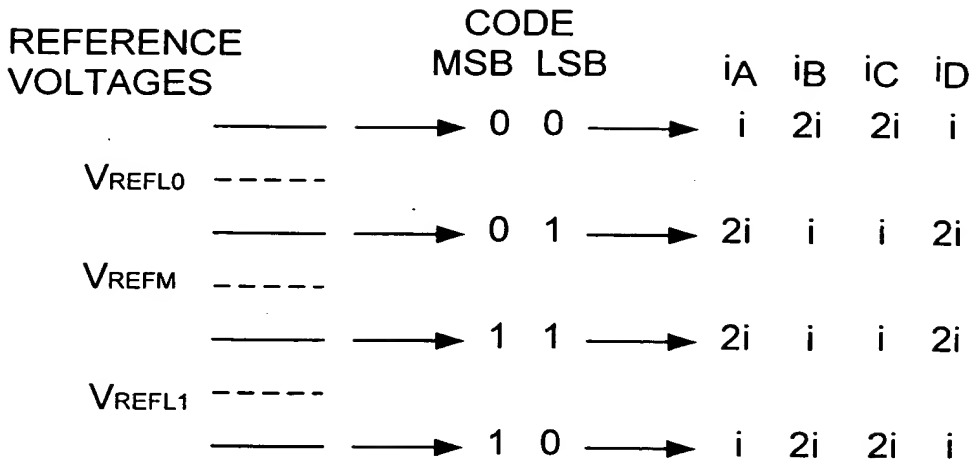

REFERENCE VOLTAGES
CODE
MSB LSB
iA iB iC iD
0 0
i 2i 2i i
VREFL0
0 1
2i i i 2i
VREFM
1 1
2i i i 2i
VREFL1
1 0
i 2i 2i i

FIG. 48

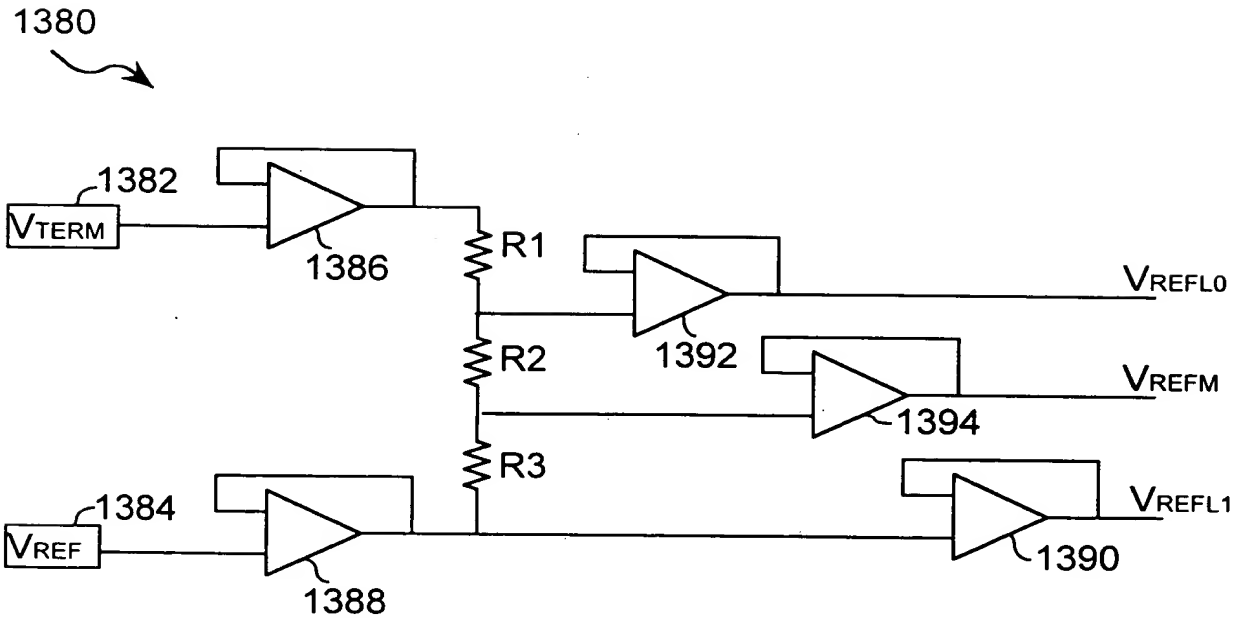

1380
1382
VTERM
1386
R1
R2
R3
1392
VREFL0
1394
VREFM
1384
VREF
1388
1390
VREFL1

FIG. 49

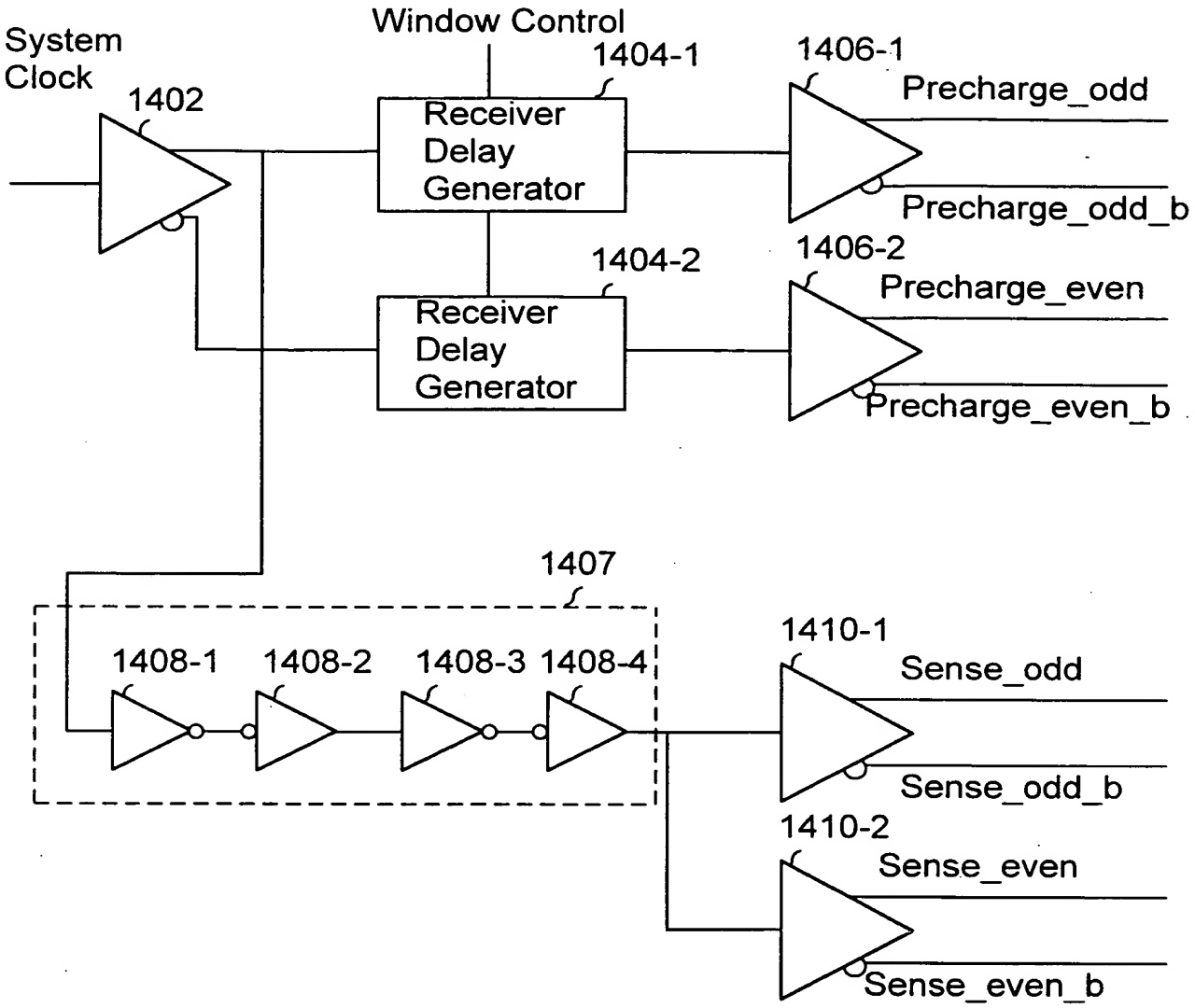
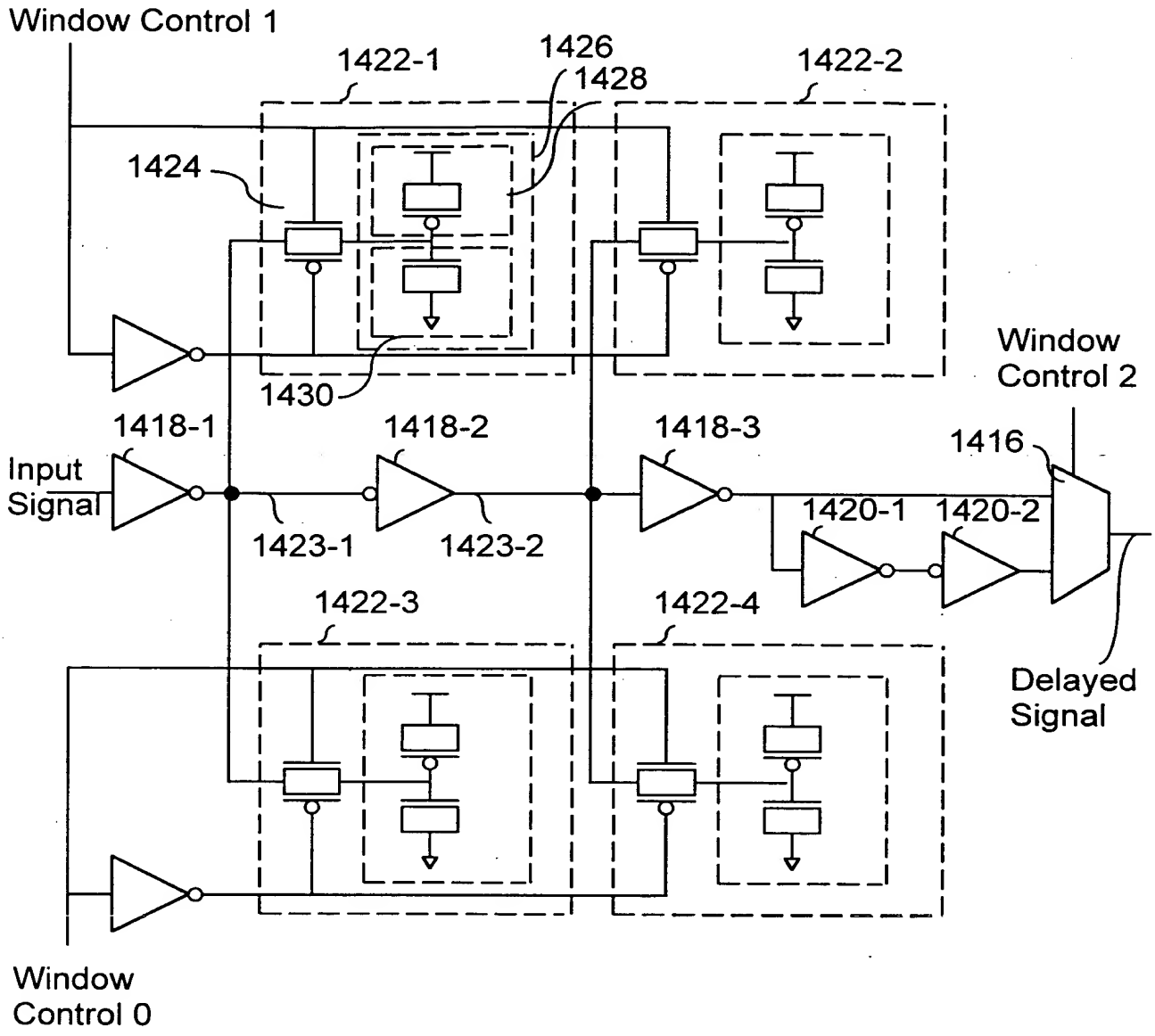

RECEIVER TIMING CIRCUIT
1116
System Clock
1402
Window Control
1404-1
Receiver Delay Generator
1404-2
Receiver Delay Generator
1406-1
Precharge_odd
Precharge_odd_b
1406-2
Precharge_even
Precharge_even_b
1407
1408-1
1408-2
1408-3
1408-4
1410-1
Sense_odd
Sense_odd_b
1410-2
Sense_even
Sense_even_b

FIG. 50



Receiver Delay Generator

FIG. 51

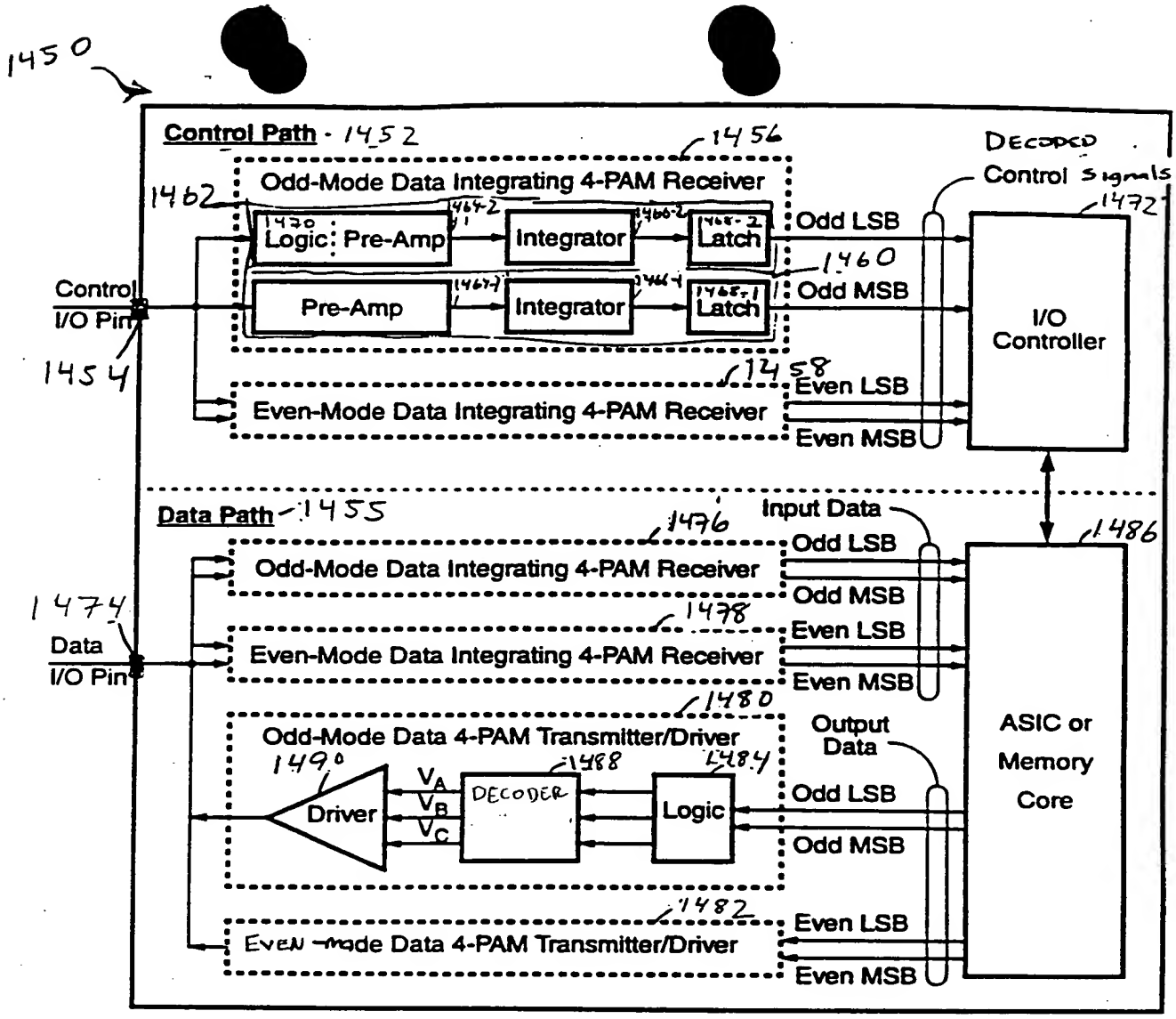

1450
Control Path - 1452
1456
Odd-Mode Data Integrating 4-PAM Receiver
1462
Logic
Pre-Amp
Integrator
Latch
Pre-Amp
Integrator
Latch
Odd LSB
Odd MSB
1460
Decoded Control Signals
1472
I/O Controller
Control I/O Pin
1454
1458
Even LSB
Even MSB
Even-Mode Data Integrating 4-PAM Receiver
Data Path - 1455
Input Data
1476
Odd LSB
Odd MSB
Odd-Mode Data Integrating 4-PAM Receiver
1486
1474
Data I/O Pin
1478
Even LSB
Even MSB
Even-Mode Data Integrating 4-PAM Receiver
1480
Odd-Mode Data 4-PAM Transmitter/Driver
Output Data
1490
Driver
V_A
V_B
V_C
DECODER
1488
Logic
1484
Odd LSB
Odd MSB
ASIC or Memory Core
1482
Even LSB
Even MSB
Even-mode Data 4-PAM Transmitter/Driver

FIG. 52A

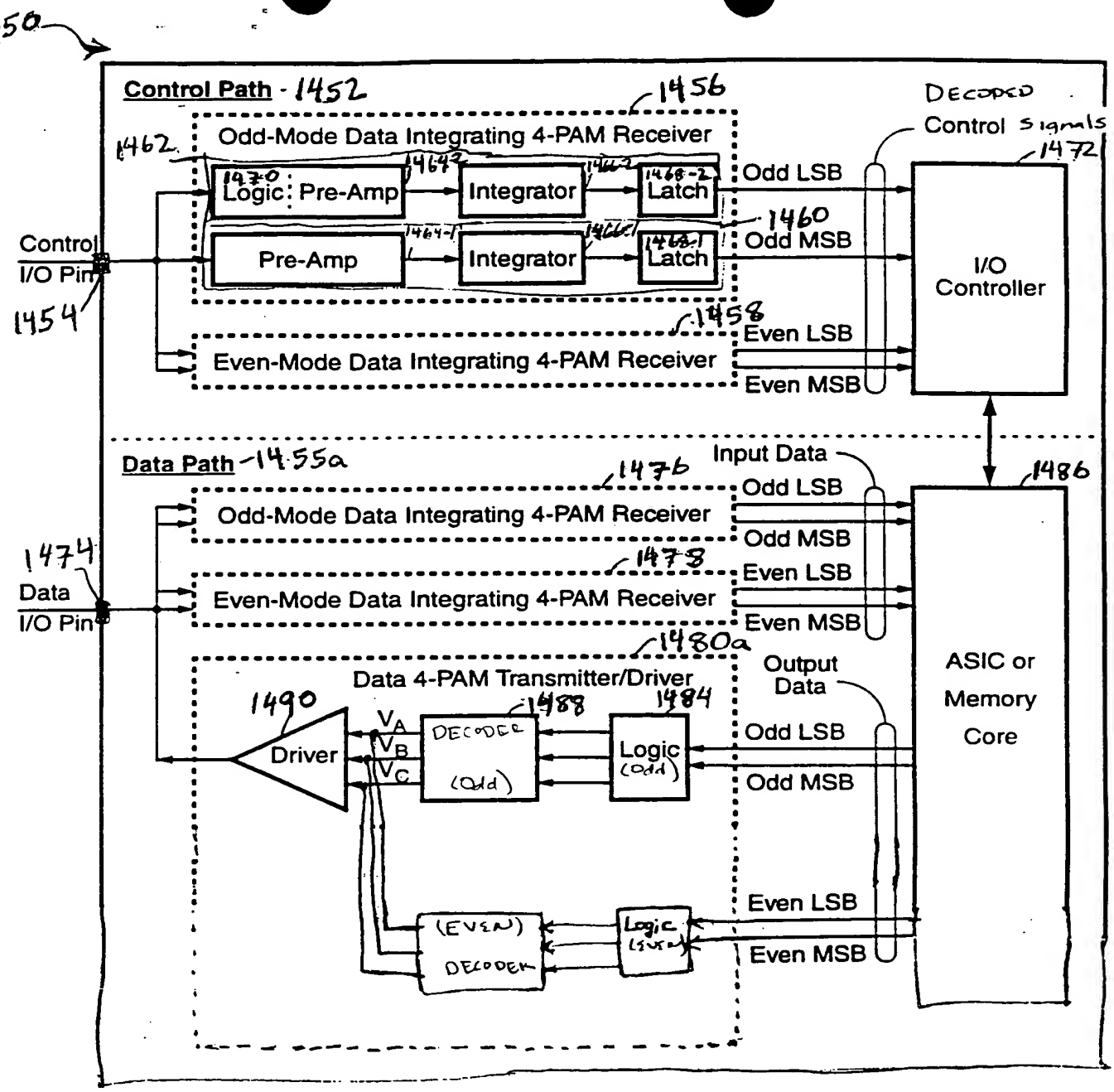
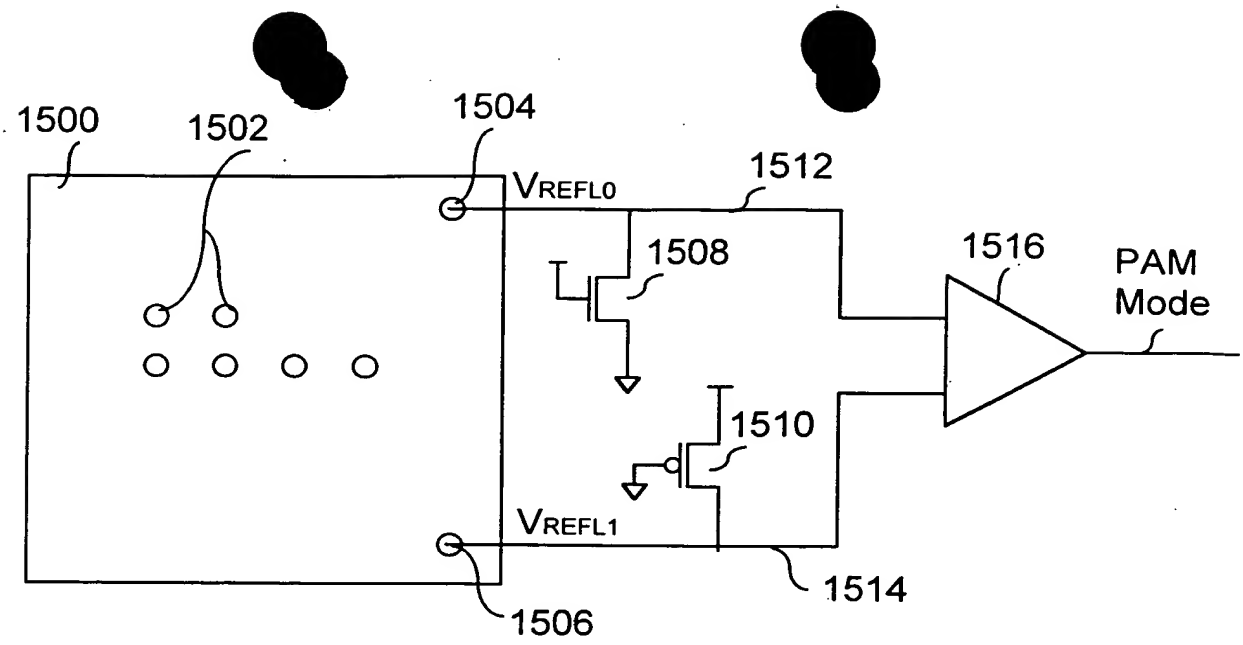

1450
Control Path - 1452
1456
Odd-Mode Data Integrating 4-PAM Receiver
1462
1470
Logic
Pre-Amp
Integrator
Latch
Pre-Amp
Integrator
Latch
Control
I/O Pin
1454
Odd LSB
Odd MSB
1460
Even LSB
Even MSB
1458
Even-Mode Data Integrating 4-PAM Receiver
Decoded
Control signals
1472
I/O
Controller
Data Path - 1455a
1476
Odd-Mode Data Integrating 4-PAM Receiver
1474
Data
I/O Pin
1478
Even-Mode Data Integrating 4-PAM Receiver
Input Data
Odd LSB
Odd MSB
Even LSB
Even MSB
1486
1480a
Data 4-PAM Transmitter/Driver
1490
Driver
VA
VB
VC
1488
DECODER
(Odd)
1484
Logic
(Odd)
(EVEN)
DECODER
Logic
Output
Data
Odd LSB
Odd MSB
Even LSB
Even MSB
ASIC or
Memory
Core

FIG. 52B



Automatic Detection of 2-PAM or 4-PAM Mode

FIG. 53

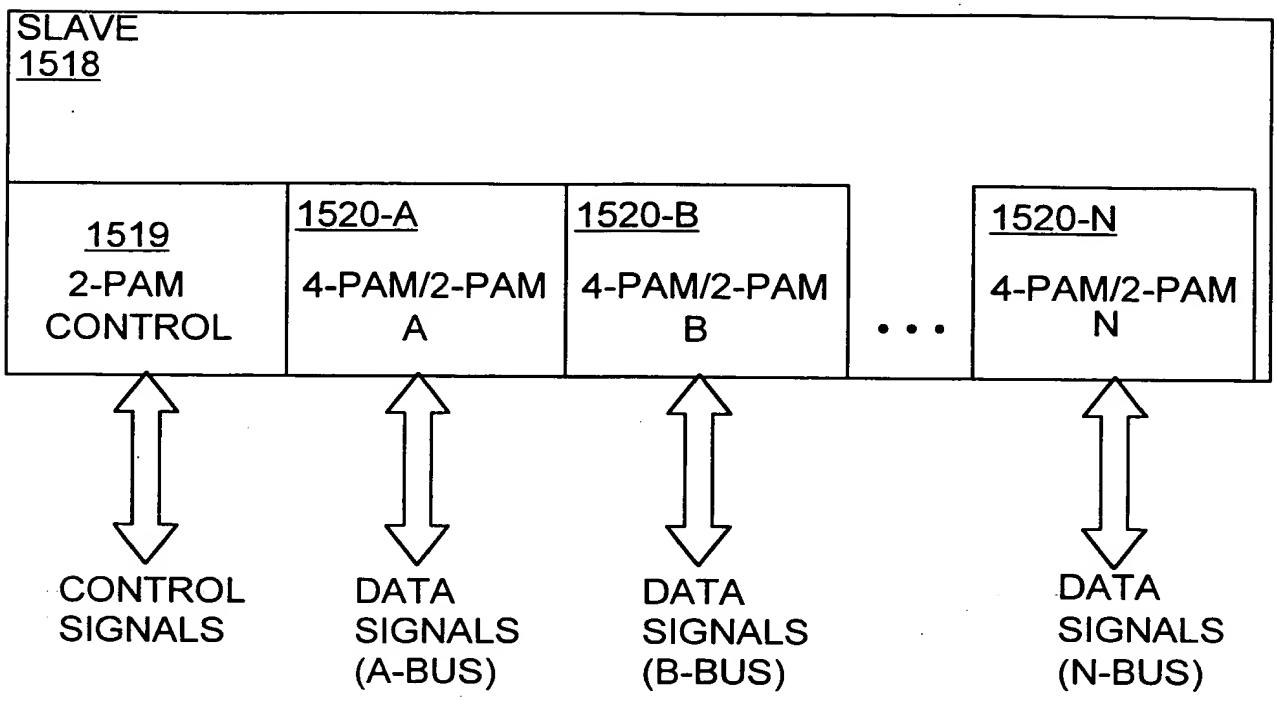


FIG. 54A

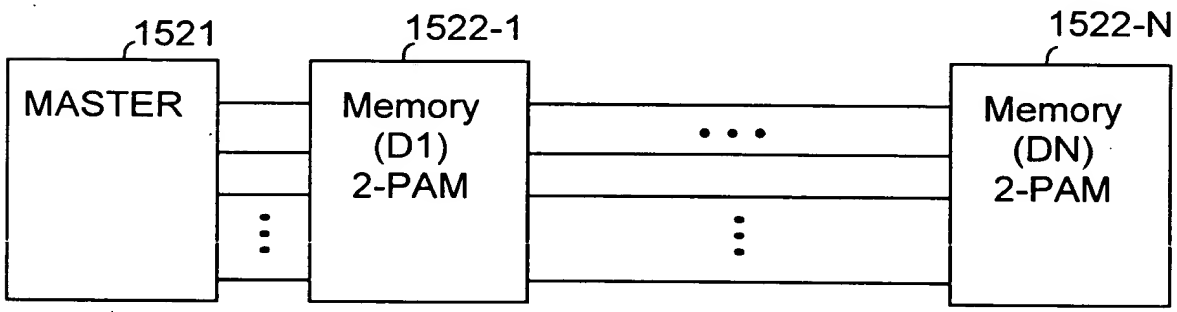


FIG. 54B

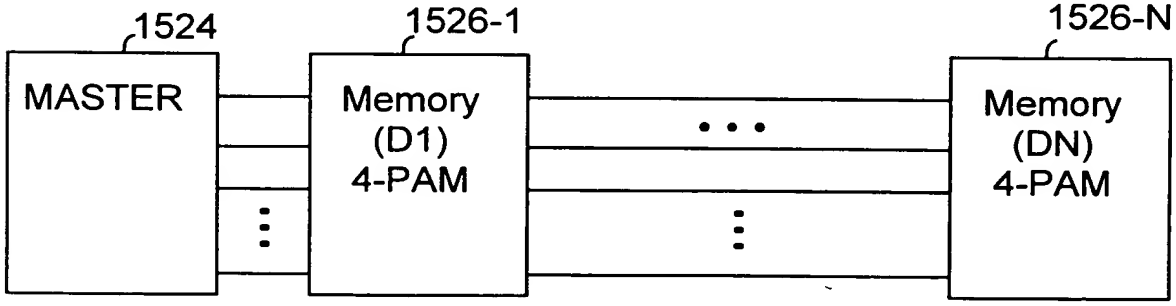
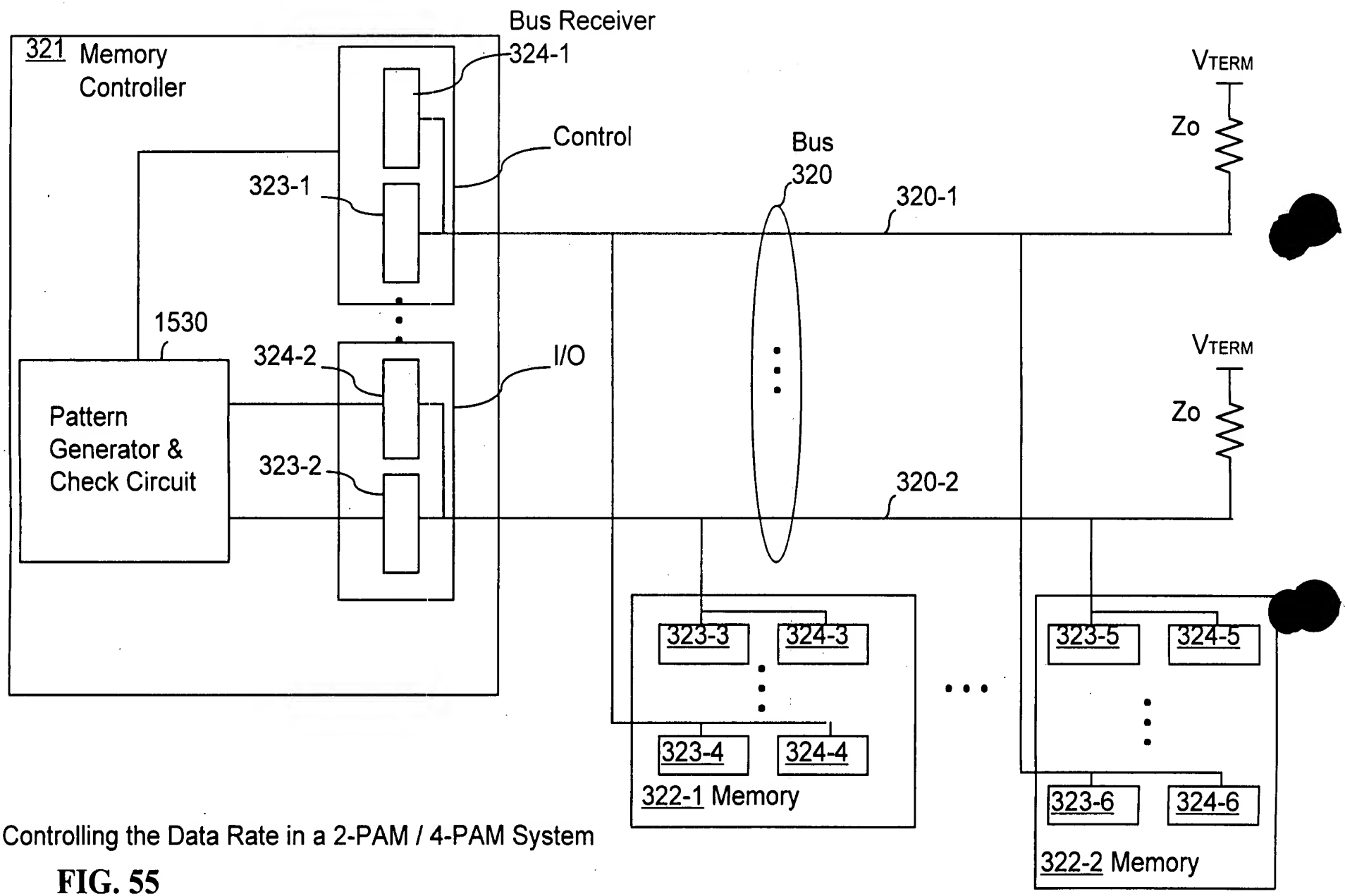
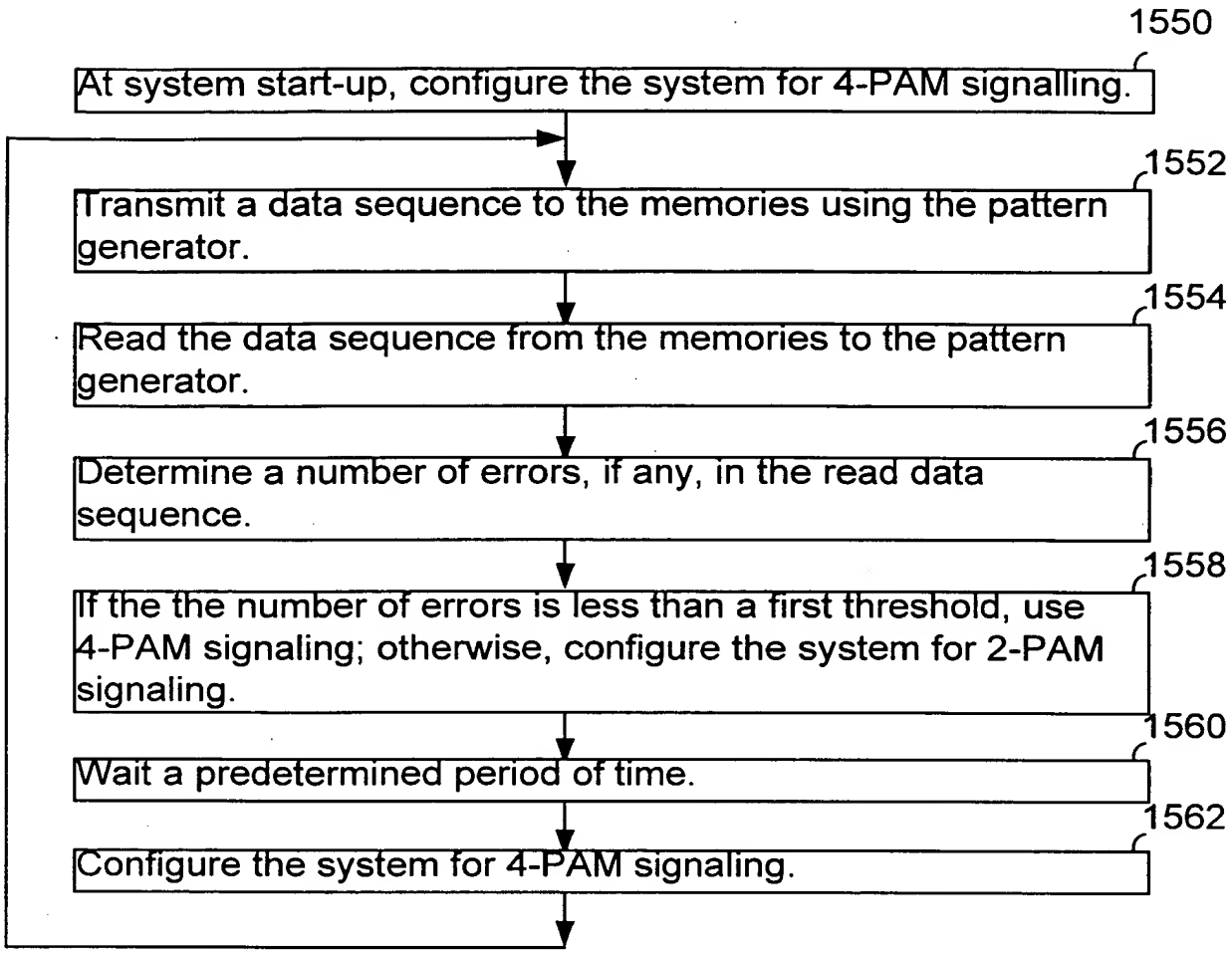


FIG. 54C



Controlling the Data Rate in a 2-PAM / 4-PAM System

FIG. 55



Method for Determining 4-PAM / 2-PAM Signalling as a Function of Error Rate

FIG. 56

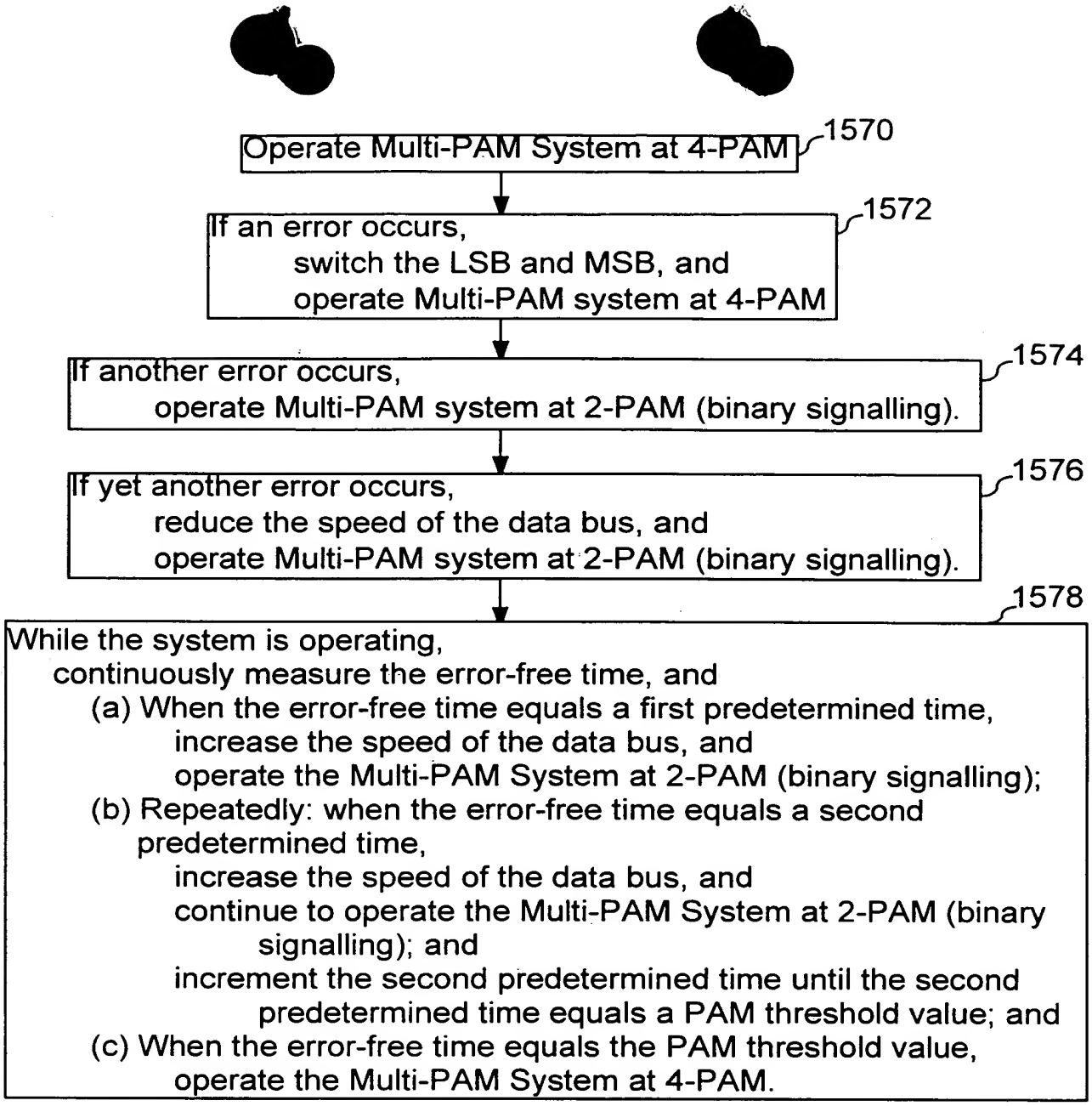

Operate Multi-PAM System at 4-PAM
1570
If an error occurs,
switch the LSB and MSB, and
operate Multi-PAM system at 4-PAM
1572
If another error occurs,
operate Multi-PAM system at 2-PAM (binary signalling).
1574
If yet another error occurs,
reduce the speed of the data bus, and
operate Multi-PAM system at 2-PAM (binary signalling).
1576
1578
While the system is operating,
continuously measure the error-free time, and
(a) When the error-free time equals a first predetermined time,
increase the speed of the data bus, and
operate the Multi-PAM System at 2-PAM (binary signalling);
(b) Repeatedly: when the error-free time equals a second predetermined time,
increase the speed of the data bus, and
continue to operate the Multi-PAM System at 2-PAM (binary signalling); and
increment the second predetermined time until the second predetermined time equals a PAM threshold value; and
(c) When the error-free time equals the PAM threshold value,
operate the Multi-PAM System at 4-PAM.

FIG. 57

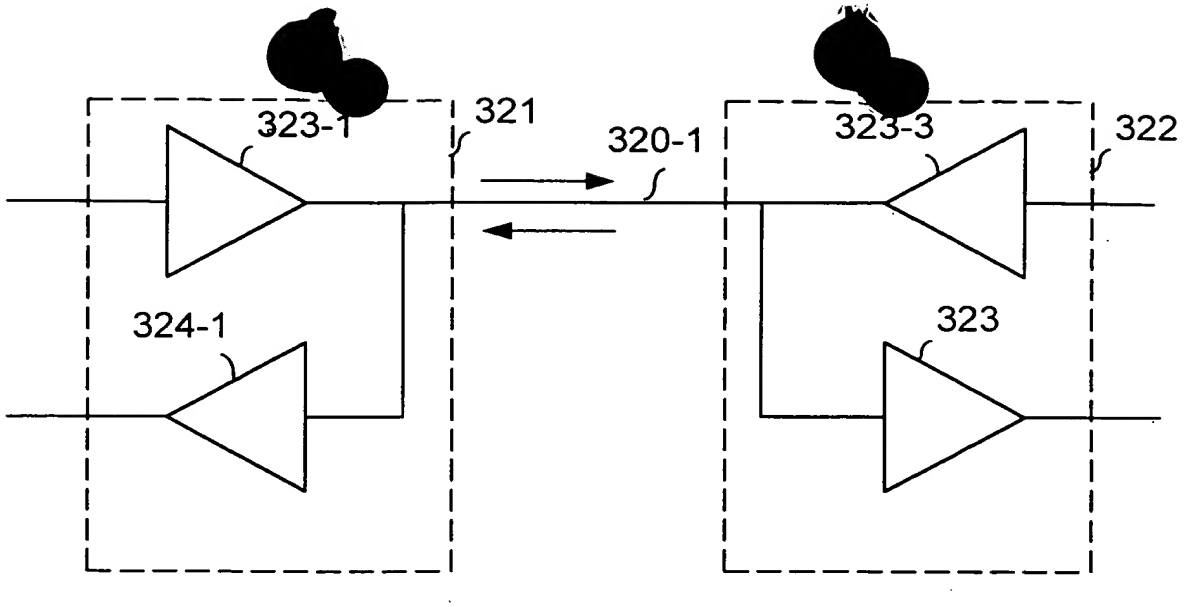

323-1
321
320-1
323-3
322
324-1
323

FIG. 58

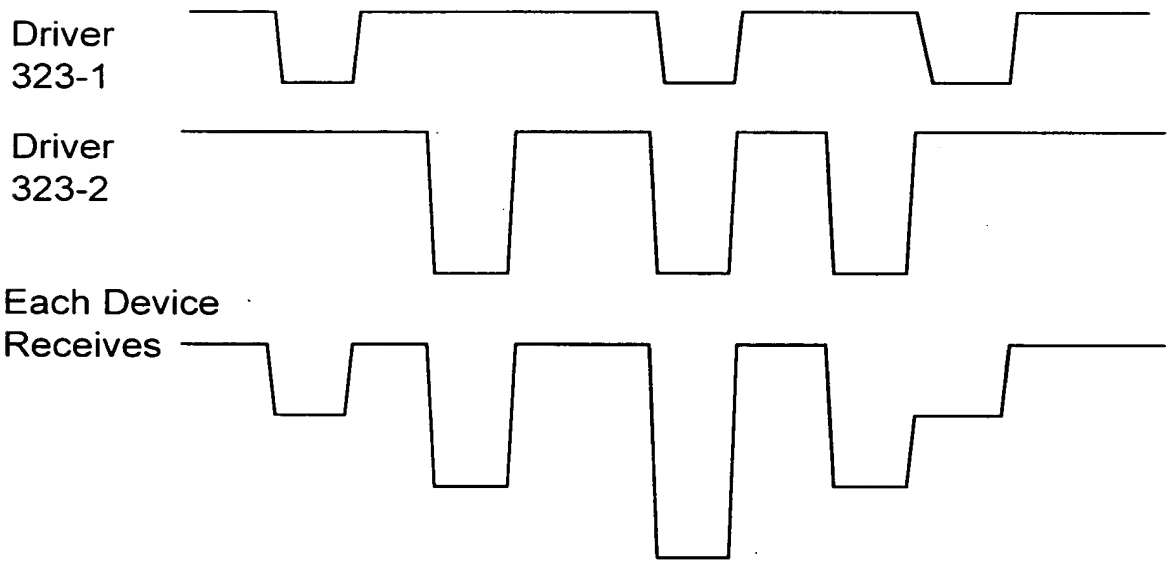

Driver
323-1
Driver
323-2
Each Device
Receives

FIG. 59

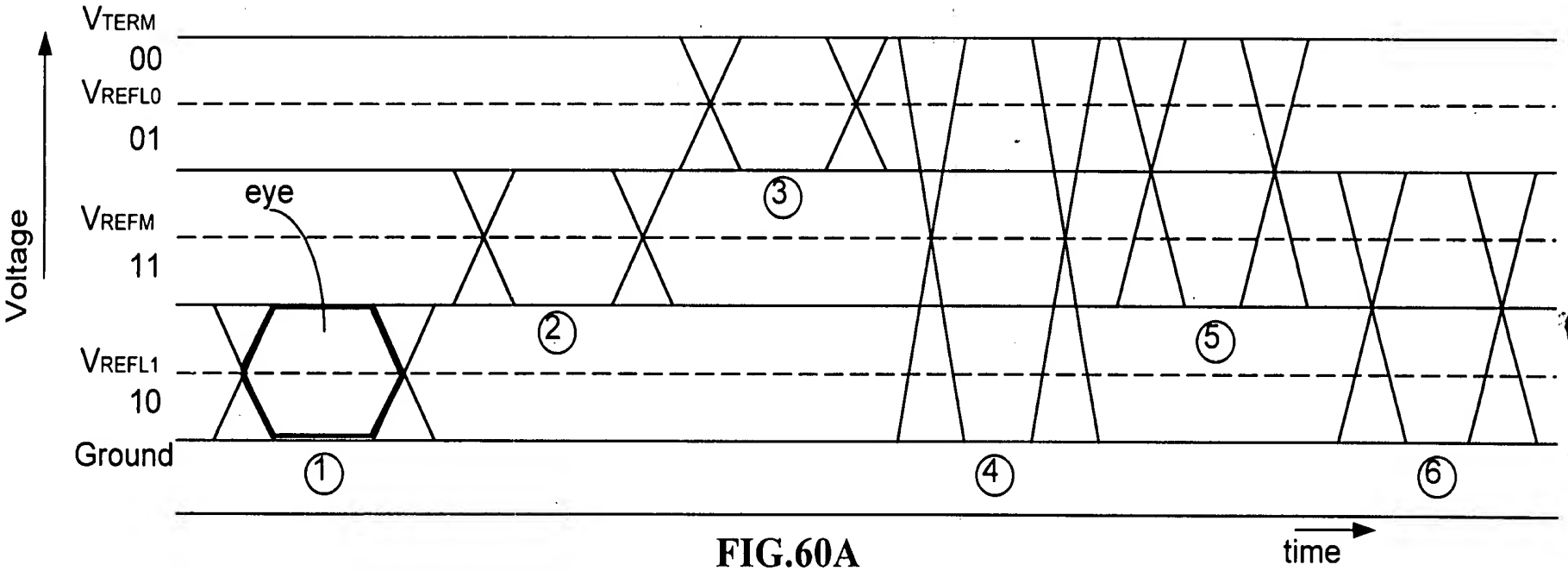


FIG.60A

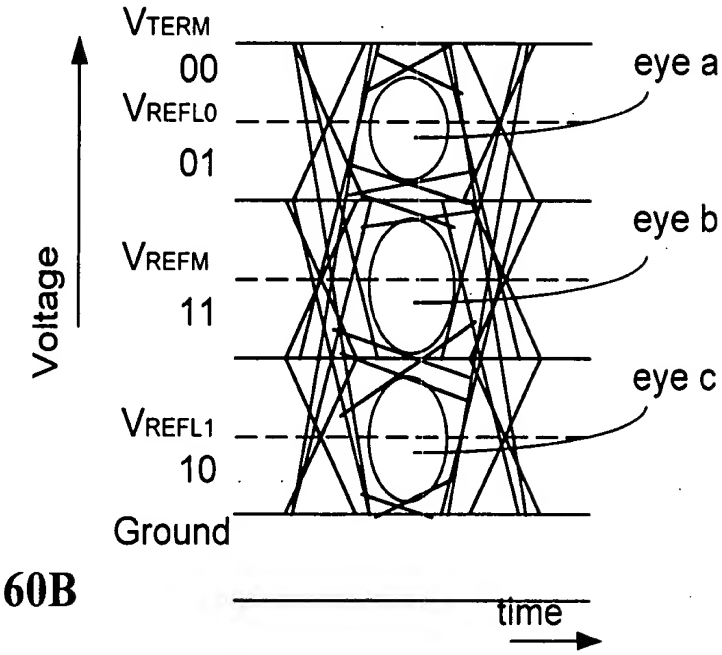


FIG. 60B